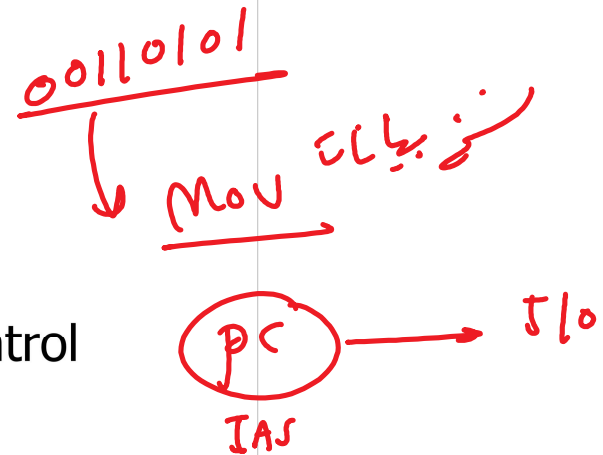


William Stallings Computer Organization and Architecture 6th Edition

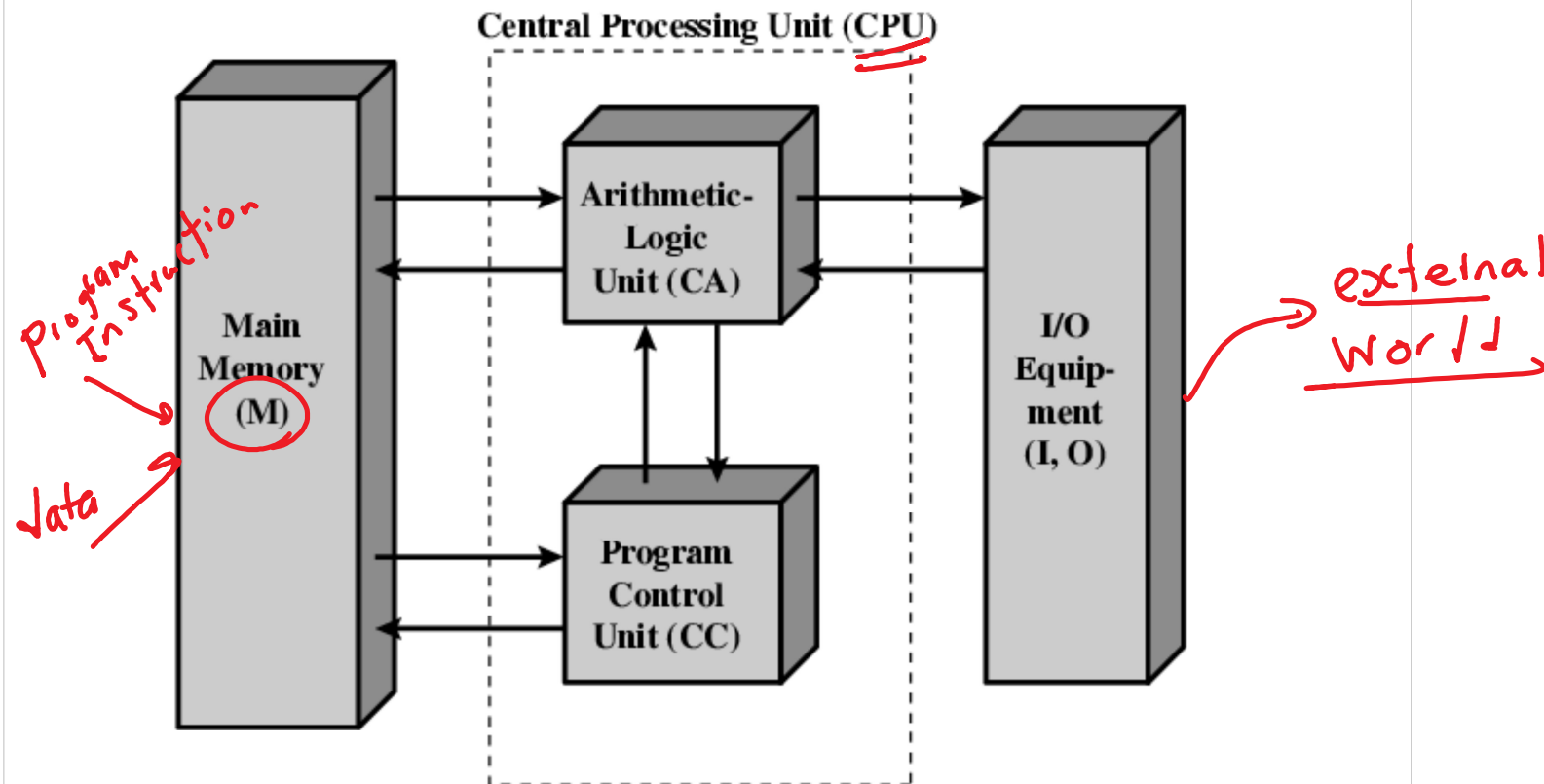
Chapter 2 Computer Evolution and Performance

von Neumann/Turing

- Stored Program concept ✓
- Main memory storing programs and data
- ALU operating on binary data
- Control unit interpreting instructions from memory and executing
- Input and output equipment operated by control unit
- Princeton Institute for Advanced Studies
 - IAS
- Completed 1952



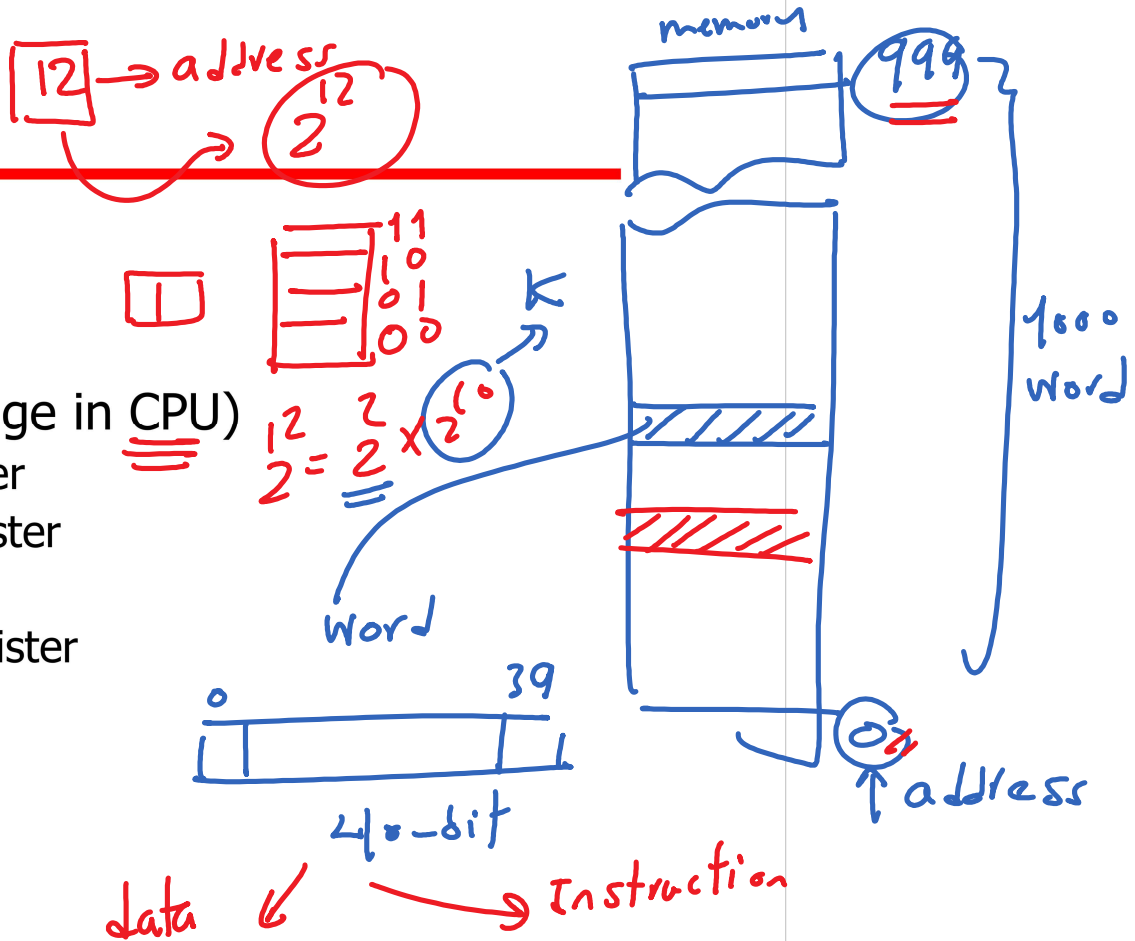
Structure of von Neumann machine



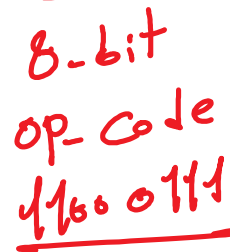
IAS - details

- 1000 x 40 bit words
 - Binary number
 - 2 x 20 bit instructions
- Set of registers (storage in CPU)
 - Memory Buffer Register
 - Memory Address Register
 - Instruction Register
 - Instruction Buffer Register
 - Program Counter
 - Accumulator
 - Multiplier Quotient

1000 $\Rightarrow$ Word



Structure of IAS – detail



Instruction Buffer Register

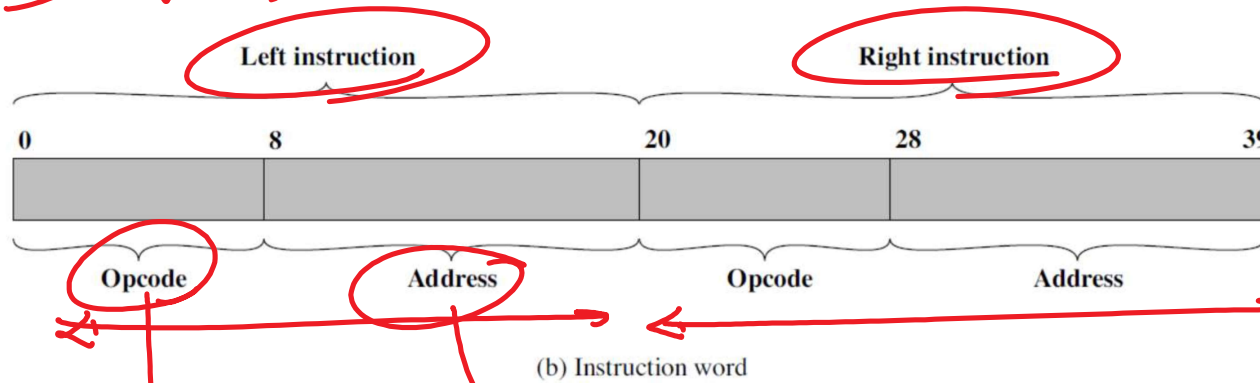
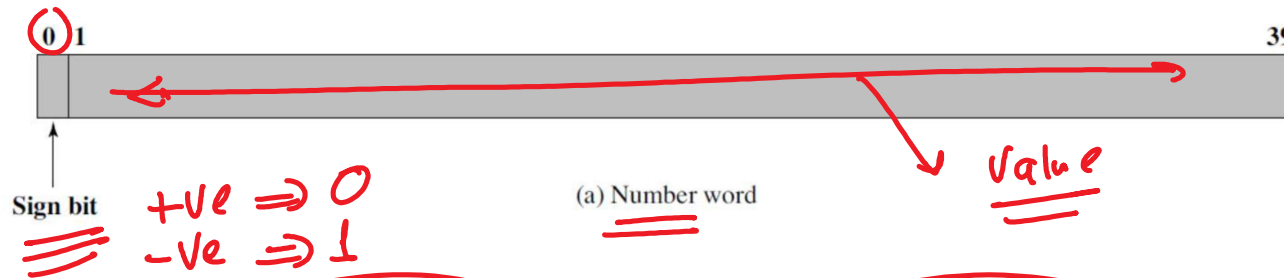
Fetch



MAR: memory
Address
Register

↳ PC
program Counter

Instruction Word



Mnemonic

MOV
ADD
SUB
MVI

12

bit

$\Rightarrow 2 \Rightarrow 4k = 4096$

Data

Instruction

IAS Registers

- **Memory buffer register (MBR):** Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit.
- **Memory address register (MAR):** Specifies the address in memory of the word to be written from or read into the MBR.
- **Instruction register (IR):** Contains the 8-bit opcode instruction being executed.
- **Instruction buffer register (IBR):** Employed to hold temporarily the right-hand instruction from a word in memory.
- **Program counter (PC):** Contains the address of the next instruction-pair to be fetched from memory.
- **Accumulator (AC) and multiplier quotient (MQ):** Employed to hold temporarily operands and results of ALU operations. For example, the result of multiplying two 40-bit numbers is an 80-bit number; the most significant 40 bits are stored in the AC and the least significant in the MQ.

IAS Architecture

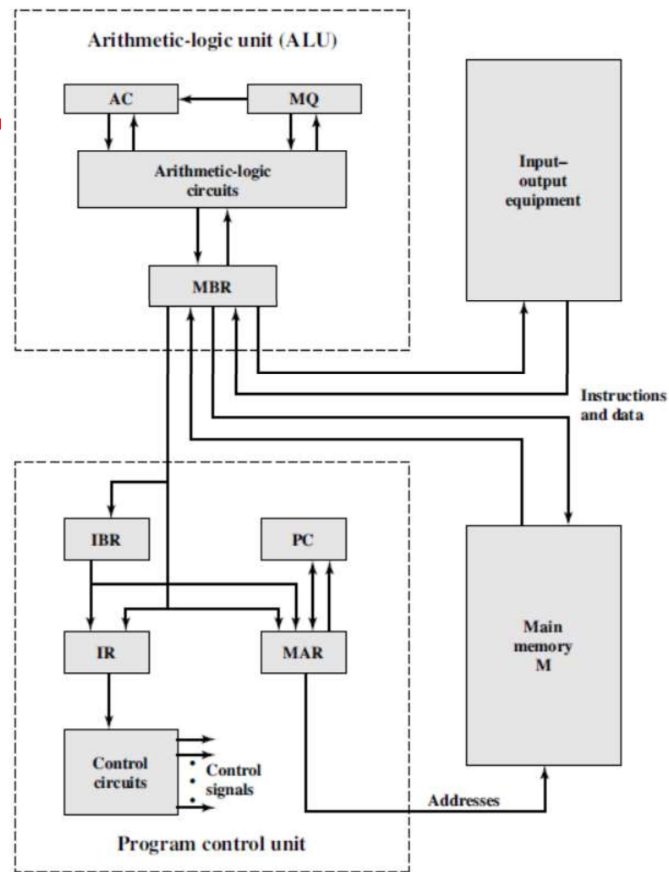


Figure 2.3 Expanded Structure of IAS Computer

Instruction Set

- The set of commands that is understood by the MP
- This is given by the **manufacturer**
- In general, the instructions are **classified** as
 - Data transfer
 - Arithmetic and logic
 - Bit manipulation
 - Loops and jumps
 - Strings
 - Subroutines and interrupts
 - Control
- The **mnemonics** codes are microprocessor – or microcontroller- specific and should be obtained from the manufacturer's data sheet

MP Basic Operation

- A microprocessor executes a program by **repeatedly cycling** through the following three steps:
 - △ **Fetch** an instruction from memory and place it in the CPU.
 - △ **Decode** the instruction; if other information is required by the instruction, fetch the other information. In the decode step, the **program counter** is updated to point to the next instruction.
 - △ **Execute** the instruction (**do what the instruction says**). Results are returned to registers and memory during this step.