Taibah University		College of Computers science and Engineering
Computer Organization and Architecture COE 224		Date: 26 April 2019
Final Exam		Total Marks: 40
Name:		ID:

Question 01 **[10 Marks]**

(A) **[5 Marks]**

Regarding the assembly program shown below— written for 8086 Microprocessor

```
1399:0100 B401          MOV     AH,01
1399:0102 CD21          INT     21
1399:0104 88C3          MOV     BL,AL
1399:0106 80CB20        OR      BL,20
1399:0109 B402          MOV     AH,02
1399:010B 88DA          MOV     DL,BL
1399:010D CD21          INT     21
1399:010F B44C          MOV     AH,4C
1399:0111 CD21          INT     21
```

1. The program will be saved to memory starting at physical address of
   a) 13A90
   b) B401
   c) 1399
   d) 0100
2. The machine code of the instruction INT 21 is
   a) CD21
   b) 0102
   c) 1399
   d) B402
3. The complete machine instruction that is saved to starting from memory address 13A96 H is
   a) 80CB20
   b) 88DA
   c) B44C
   d) B402
4. The instruction OR BL,20 is _____ Byte (s) Instruction
   a) One
   b) Two
   c) Three
   d) zero
5. The end of the program is at effective address equal to
   a) 1399
   b) 0111
   c) 010F
   d) 0112
6. What is the function of the first INT
   a) Read character
   b) Print character
   c) Print message
   d) halt
7. After executing the 8th instruction, AH register =
   a) 4C
   b) BL
   c) 02
8. The instruction, **MOV AX, 0005H** belongs to the address mode
   a) Register
   b) Direct
   c) Immediate
   d) Register relative
9. The instruction, MOV AX, [2500H] is an example of
   a) Immediate addressing mode
   b) Direct addressing mode
   c) Indirect addressing mode
   d) Register addressing mode
10. The instruction, MOV AX,[BX] is an example of
    a) Direct addressing mode
    b) Register addressing mode
    c) Register indirect addressing mode
    d) None of the above

(B) **[5 Marks]**

(a) Find the memory address of the next instruction executed by the microprocessor for the following **CS:IP** combinations:
CS = 5000H and IP = 2000H
$PA = CS \times 10 + IP$
$PA = 50000 + 2000 = 52000H$

(b) A **code segment** is to be located from address **B0000** to **BFFFF**. What value must be loaded into **CS?**
DS = B000

(c) Write a program to subtract a hex number in offset address **0055H** from a hex number in offset address **0065H** and store the result to location addressed by offset address **0070H**
MOV AX,[0065]
SUB AX, [0055]
MOV [0070],AX

(d) If the current values in the **code segment register** and the **instruction pointer** are **0200** and **01AC**, respectively, what **physical address** is used in the next instruction fetch?
$PA = CS \times 10 + IP$
$PA = 2000 + 01AC = 21ACH$

Question 2: **[10 Marks]**

(A) **[5 Marks]**

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder contains the immediate operand or an operand address.

(a) What is the maximum directly addressable memory capacity (in bytes)?

Op-code	Immediate operand/ operand address
8-bit	24-bit

Address = 24-bit

Memory = $2^{24} = 16$ MByte

(b) How many bits are needed for the program counter and the instruction register?

PC = 24-bits

IR = 8//32 bits

How many instructions are there in the instruction set of this processor?

$\#\ instructions\ =\ 2^8 = 256$ instructions

(B) **[5 Marks]**

Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:

INPR: Input Register, 8 bits

OUTR: Output Register, 8 bits

FGI: Input Flag, 1 bit

FGO: Output Flag, 1 bit

IEN: Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.

(a) Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.

Input from the Teletype is stored in INPR. The INPR will only accept data from the Teletype when FGI=0. When data arrives, it is stored in INPR, and FGI is set to 1. The CPU periodically checks FGI. If FGI =1, the CPU transfers the contents of INPR to the AC and sets FGI to 0. When the CPU has data to send to the Teletype, it checks FGO. If FGO = 0, the CPU must wait. If FGO = 1, the CPU transfers the contents of the AC to OUTR and sets FGO to 0. The Teletype sets FGI to 1 after the word is printed

(b) Describe how the function can be performed more efficiently by also employing IEN

The process described in (a) is very wasteful. The CPU, which is much faster than the Teletype, must repeatedly check FGI and FGO. If interrupts are used, the Teletype can issue an interrupt to the CPU whenever it is ready to accept or send data. The IEN register can be set by the CPU (under programmer control)

Question 3: **[10 Marks]**

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine

(a) How is a 16-bit memory address divided into tag, line number, and byte number?

Address = 16 bits w = 3 bits

No. of line = $32 = 2^5$ r = 5

Tag bits = 16 – 3 – 5 = 8

Tag	Line	Word
8	**5**	**3**

(b) Into what line would bytes with each of the following addresses be stored?

1010 1010 1010 1010

Line bits 1010 1

Line number = **21**

(c) How many total bytes of memory can be stored in the cache?

$Cache\ size\ =\ No.of\ line \times Block\ size$

$Cache\ size = 2^5 \times 2^3 = 2^8 = 256\ Bytes$

(d) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

0001 1010 0001 1**000** through 0001 1010 0001 1**111**

Question 4: **[10 Marks]**

(a) Consider the page stream of page requests. **1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2:** Determine the **hit ratio *h*** for this stream using the **Least Frequently Used LFU "Optimum"** replacement policy, assume the main memory can hold **three pages** and initially all of them are vacant

1	2	3	4	2	1	5	6	2	1	2	
	1	1	1	1			1	1			
	-	2	2	2			2	2			
			3	4			5	6			

(b) A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count: Determine the effective **CPI**, **MIPS** rate, and **execution time** for this program.

Instruction Type	Instruction Count	Cycles per instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

$$Average\ CPI = \frac{45*1+32*2+15*2+8*2}{100} = \frac{155}{100} = \mathbf{1.55}$$

$$T\ =\ I_c \times CPI \times \tau$$

$$T = 100{,}000 \times 1.55 \times \frac{1}{40 \times 10^6} = \mathbf{3.875\ ms}$$

$$MIPS = \frac{f}{CPI \times 10^6} = \frac{40 \times 10^6}{1.55 \times 10^6} = \mathbf{25.8}$$

(c) Given that: Cache **access time Tc = 100 ns**, **Memory access time Tm = 500 ns**, If the effective access time is 10% greater than the cache access time, **what is the hit ratio *h***?

$$T_A = hT_c + (1-h)(T_c + T_m)$$
$$110 = 100h + 600(1-h)$$
$$1.1 = h + 6 - 6h$$
$$4.9 = 5h$$
$$h = \frac{4.9}{5} = 98\%$$