



Final Exam

Academic Year 1447 - First Semester

Exam Information معلومات الامتحان		
Course name	تصميم المنطق الرقمي	اسم المقرر
Course Code	COE 211	رمز المقرر
Exam Date	5 / 1 / 2025	التاريخ
Exam Time	11:00 – 13:00	وقت الامتحان
Exam Duration	2 Hour	مدة الامتحان
Classroom No.	GF 1	رقم قاعة الاختبار
Instructor Name	Prof. Dr. Mostafa Elhosseini	اسم استاذ المقرر
Student Information معلومات الطالب		
Student's Name		اسم الطالب
ID number		الرقم الجامعي
Section No.		رقم الشعبة
Serial Number		الرقم التسلسلي

General Instructions:

تعليمات عامة:

- Your Exam consists of 4 PAGES (except this paper) (عدد صفحات الامتحان 4 صفحة. (باستثناء هذه الورقة)
- Phones and smart devices are forbidden inside the hall. (يمنع استخدام الهواتف والأجهزة الذكية داخل القاعة.)

هذا الجزء خاص بأستاذ المادة

#	Course Learning Outcomes (CLOs)	Related Question (s)	Points	Final Score
1	Write numbers in various number systems.	Q1 – Part A	2	
2	Recognize the basics of Boolean algebra.	Q1 – Part B	2	
3	Describe the basic concept of sequential circuit.	Q1 – Part C	6	
4	Analyze small- and medium-scale logic functions as building blocks.	Q2 – Part A	6	
5	Analyze and design the behavior of sequential circuits.	Q2 – Part B	8	
6	Simplify Boolean functions using Boolean algebra and the Karnaugh map.	Q1 – Part D	8	
7	Communicate effectively in oral and written form	Q3	8	

Part A: Points 2

CLO #1

- What is the decimal equivalent of the binary number 101101_2 ?
A) 41
B) 43
C) 45
D) 47
- Which of the following represents the hexadecimal equivalent of 1110_2 ?
A) A
B) C
C) D
D) E

Part B: Points 2

CLO #2

- If $F = A(\bar{A} + B)$ then the simplified form of F is:
A) AB
B) $A + B$
C) B
D) 0
- Which expression is logically equivalent to $A \oplus B$ (XOR)?
A) $AB + \bar{A}\bar{B}$
B) $A + B$
C) $A\bar{B} + \bar{A}B$
D) $(A + B)(\bar{A} + \bar{B})$

Part C: Points 6

CLO #3

- Which of the following elements is essential in a sequential circuit but not in a combinational circuit?
A) Logic gates
B) Flip-flops
C) Boolean expressions
D) Multiplexers
- For a **D flip-flop**, the next state is given by:
A) $Q(t + 1) = D \oplus Q(t)$
B) $Q(t + 1) = D$
C) $Q(t + 1) = \bar{D}$
D) $Q(t + 1) = D \cdot Q(t)$

- For a JK flip-flop, when $J = K = 1$, the output:
A) Remains unchanged
B) Is reset to 0
C) Is set to 1
D) Toggles its current state
- A flip-flop must change state from $Q(t) = 1 \rightarrow Q(t + 1) = 0$. Which **JK inputs** can achieve this transition?
A) $J=X, K=0$
B) $J=0, K=X$
C) $J=1, K=X$
D) $J=X, K=1$
- Which signal synchronizes state changes in synchronous sequential circuits?
A) Enable
B) Reset
C) Clock
D) Data
- Which of the following is an example of a sequential circuit?
A) Full adder
B) Decoder
C) Counter
D) Multiplexer

Part D: Points 8

CLO #6

- Simplify the Boolean expression: $A + A \cdot B$
A) A
B) B
C) $A + B$
D) AB
- Using De Morgan's theorem, the complement of $A + B$ is:
A) $\bar{A} + \bar{B}$
B) AB
C) $\bar{A}\bar{B}$
D) $A\bar{B}$
- How many cells are there in a 3-variable Karnaugh map?
A) 4
B) 6
C) 8
D) 16
- Simplify the expression: $AB + A\bar{B}$
A) B
B) A

C) $A + B$

D) $\bar{A}$

15. The simplified form of $\bar{A}\bar{B} + AB$ is:

A) A

A) B

B) $\bar{A}$

C) $A + B$

16. Simplifying the Boolean function: $F = AB + \bar{A}B + ABC$ using Karnaugh map gives

A) AB

B) B

C) $A + B$

D) BC

17. What is the **minimal SOP expression** for $F(A, B, C) = \sum m(1, 3, 5, 7)$

A) C

B) AB

C) $A + C$

D) $B + C$

18. The Boolean function is defined as: $F(A, B, C) = \sum m(0, 2, 3, 6, 7)$ What is the **minimal SOP expression** for F ?

A) $B + \bar{A}\bar{C}$

B) $A + B$

C) $B + \bar{A}$

D) $AB + \bar{A}C$

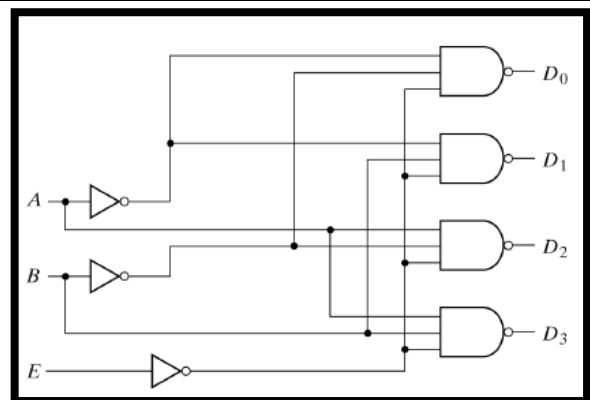
Question 2: Points: 14

CLO #4,5

Part A: Points 6

CLO #4

For the logic circuit shown below, write down the Boolean equations for outputs and then Construct the truth table



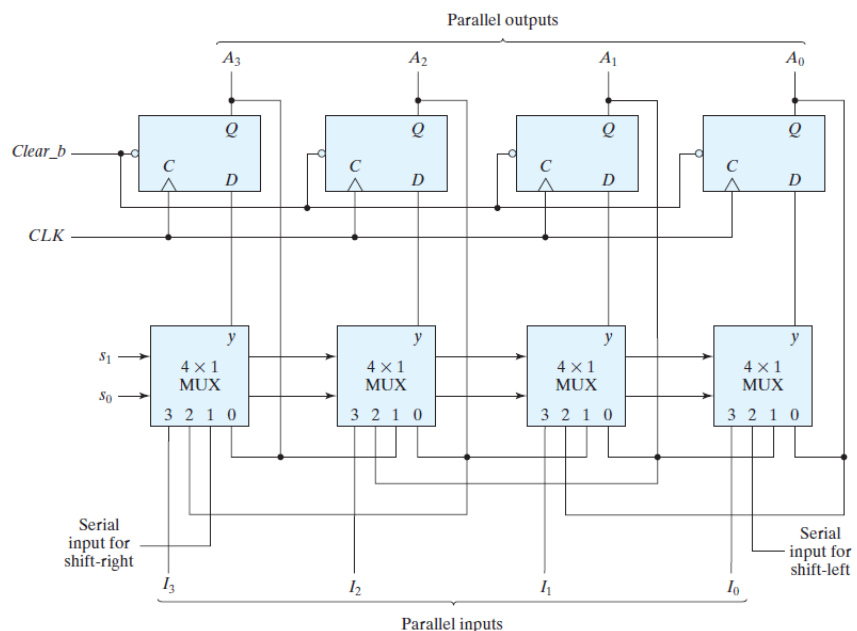
For the state table shown below, a synchronous sequential circuit is implemented using **two JK flip-flops**, where flip-flop **A** stores the state variable **A** and flip-flop **B** stores the state variable **B**;

- Using the **JK excitation table**, determine and fill in the required flip-flop inputs
- Use the completed table to **draw the corresponding state diagram**

Present State		Input x	Next State		Flip-Flop Inputs			
A	B		A	B	J_A	K_A	J_B	K_B
0	0	0	0	1				
0	0	1	0	0				
0	1	0	1	1				
0	1	1	1	0				
1	0	0	1	1				
1	0	1	1	0				
1	1	0	0	0				
1	1	1	1	1				

Question 3: Points: 8**CLO #7**

Describe the **functions** performed by this shift register, clearly explaining each mode of operation (such as holding data, shifting left, shifting right, and parallel loading).



Name

ID

Class

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1 (A) (B) (C) (D) 10 (A) (B) (C) (D)

2 (A) (B) (C) (D) 11 (A) (B) (C) (D)

3 (A) (B) (C) (D) 12 (A) (B) (C) (D)

4 (A) (B) (C) (D) 13 (A) (B) (C) (D)

5 (A) (B) (C) (D) 14 (A) (B) (C) (D)

6 (A) (B) (C) (D) 15 (A) (B) (C) (D)

7 (A) (B) (C) (D) 16 (A) (B) (C) (D)

8 (A) (B) (C) (D) 17 (A) (B) (C) (D)

9 (A) (B) (C) (D) 18 (A) (B) (C) (D)

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