College of Computer Science & Engineering at Yanbu.

جامعة طيبة
TAIBAH UNIVERSITY

كلية علوم وهندسة الحاسبات بينبع

Department of Computer Science.

قسم علوم الحاسبات

Final Exam

Academic Year 1447 - Second Semester

Exam Information معلومات الامتحان			
Course name	**تنظيم وبناء الحاسب**		**اسم المقرر**
Course Code	**COE 224**		**رمز المقرر**
Exam Date	7 / 6 / 2026	**الأحد**	**تاريخ الامتحان**
Exam Time	8:30 – 10:30		**وقت الامتحان**
Exam Duration	2 Hour		**مدة الامتحان**
Classroom No.	**GF 1**		**رقم قاعة الاختبار**
Instructor Name	**Prof. Dr. Mostafa Elhosseini**		**اسم استاذ المقرر**

Student Information معلومات الطالب		
Student's Name		**اسم الطالب**
ID number		**الرقم الجامعي**
Section No.		**رقم الشعبة**
Serial Number		**الرقم التسلسلي**

General Instructions:

تعليمات عامة:

- Your Exam consists of 4 PAGES (except this paper)
- Phones and smart devices are forbidden inside the hall.

- عدد صفحات الامتحان 4 صفحة. (بإستثناء هذه الورقة)
- يمنع استخدام الهواتف والأجهزة الذكية داخل القاعة.

هذا الجزء خاص بأستاذ المادة

This section is ONLY for instructors.

#	Course Learning Outcomes (CLOs)	Related Question (s)	Points	Final Score
1	Describe the instruction set architecture of a MIPS processor	Q1	8	
2	Describe the organization/operation of memory and caches	Q2	8	
3	Describe the organization/operation of Input/Output devices	Q3	8	
4	Analyze, develop, and test MIPS assembly language programs	Q4	8	
5	Design the datapath of a single-cycle processor	Q5	8	

Question 1: Points: 8		CLO #1

For **MIPS Architecture**, answer the following MCQs.

1. MIPS as a processor architecture follows which design philosophy?
   A. CISC
   B. VLIW
   C. Harvard-only
   D. RISC
2. The acronym MIPS originally stood for:
   A. Microprocessor without Interlocked Pipeline Stages
   B. Microprocessor Integrated Processing System
   C. Memory Integrated Processing Structure
   D. Machine Instruction Processing Speed
3. When MIPS is used as a performance metric, it stands for:
   A. Microprocessor Integrated Performance System
   B. Maximum Internal Processing Speed
   C. Memory Instructions Per Segment
   D. Million Instructions Per Second
4. Which of the following is TRUE about MIPS architecture?
   A. Instructions have variable length
   B. Arithmetic operations access memory directly
   C. It uses only 8 registers
   D. All instructions are 32 bits long
5. In MIPS architecture, arithmetic operations are performed:
   A. Between registers only
   B. Directly on memory
   C. Only using immediate values
   D. Only on stack
6. In MIPS, to access A[8], the correct offset is:
   A. 8
   B. 16
   C. 32
   D. Depends on compiler
7. Why is **addi** preferred overloading a constant from memory?
   A. It reduces register usage
   B. It uses fewer bits in instruction
   C. It allows floating-point operations
   D. It avoids memory access and improves speed
8. Which operation requires more cycles (in general)?
   A. add $s1,$s2,$s3
   B. addi $s1,$s2,5
   C. and $s1,$s2,$s3
   D. lw $s1,20($s2)

Question 2: Points: 8		CLO #2

9. Cache Memory acts between
   A. RAM and ROM
   B. CPU and hard disk
   C. CPU and main memory
   D. RAM and I/O
10. To speed up the performance of the processor is used
   A. Timer
   B. Clock signal
   C. Pipelining
   D. Memory
11. Which of the following is fastest?
   A. Cache (SRAM)
   B. Main memory (DRAM)
   C. Hard disk
   D. Optical disk
12. Why is SRAM more expensive than DRAM?
   A. It consumes more power
   B. It requires more transistors per bit
   C. It needs refresh circuitry
   D. It is non-volatile

For the memory locations in the next table, write MIPS code to **sort the data from lowest to highest**, placing the lowest value in the smallest memory location. Use a minimum number of MIPS instructions. Assume the base address of Array is stored in register **$s6**.

```
lw  $t0, 24($s6)      # $t0 = 2
lw  $t1, 28($s6)      # $t1 = 4
lw  $t2, 36($s6)      # $t2 = 6
lw  $t3, 40($s6)      # $t3 = 1

sw  $t3, 24($s6)      # Array[24] = 1
sw  $t0, 28($s6)      # Array[28] = 2
sw  $t1, 36($s6)      # Array[36] = 4
sw  $t2, 40($s6)      # Array[40] = 6
```

The table below shows 32-bit values of an array stored in memory.

Address	Data
24	2
28	4
32	3
36	6
40	1

Question 3: Points: 8		**CLO #3**

A. Describe the three main types of buses involved in I/O communication.

The three main types of buses involved in I/O communication are the address bus, data bus, and control bus.

The address bus carries the address of the memory location or I/O device that the CPU wants to access. When the CPU performs an input or output operation, it places the device or memory address on the address bus to select the correct destination.

The data bus carries the actual data being transferred between the CPU, memory, and I/O devices. It is bidirectional because data can move both to and from the CPU.

The control bus carries control and timing signals that coordinate the operation. These signals include read, write, interrupt request, interrupt acknowledgment, and bus request signals. The control bus ensures that all components act at the correct time and in the correct direction.

B. Explain the impact of increasing the size (width) of the address bus and the data bus in a computer system. Discuss how each affects system performance and capacity.

Increasing the width of the address bus increases the maximum amount of memory that the system can address.

Increasing the width of the data bus increases the amount of data that can be transferred in a single clock cycle. A wider data bus improves data throughput because more bits are moved at once between the CPU, memory, and I/O devices. This can enhance system performance, particularly in memory-intensive applications.

Question 4: Points: 8		CLO #4

For **MIPS Architecture**, answer the following MCQs.

13. What is the value of $t2?

```
li $t0, 10
li $t1, 4
sub $t2, $t0, $t1
```

A. 14
B. -6
C. 6
D. 40

14. What is the output?

```
li $a0, 7
li $v0, 1
syscall
```

A. 7
B. 0
C. 1
D. Error

15. What does **j** label do?
A. Conditional jump
B. Function call
C. Load address
D. Unconditional jump

16. Which instruction **loads a word from memory**?
A. sw
B. lw
C. la
D. li

17. In MIPS, how can you implement **NOT $t1**?
A. and $t0, $t1, $t1
B. nor $t0, $t1, $zero
C. or $t0, $t1, $zero
D. xor $t0, $t1, $t1

18. What is the result of:

```
li $t0, 0b1101
li $t1, 0b0101
and $t2, $t0, $t1
```

A. 1111
B. 1001
C. 0101
D. 0001

19. What is the purpose of using **AND** in:
and $t0, $t1, 0xFF
A. Flip bits
B. Clear upper bits
C. Add numbers
D. Shift left

20. Which instruction **sets the lowest bit of $t0 to 1**?
A. and $t0, $t0, 1
B. or $t0, $t0, 1
C. xor $t0, $t0, 1
D. nor $t0, $t0, 1

Question 5: Points: 8		CLO #5

21. Which datapath component decides between multiple input sources?
A. ALU
B. Multiplexer (MUX)
C. Register File
D. Instruction Memory

22. In the datapath, the instruction memory is primarily used to:
A. Store data values
B. Store program instructions
C. Perform computations
D. Control signals

23. In a load word (**lw**) instruction, which unit calculates the memory address?
    A. Register File
    B. ALU
    C. Instruction Memory
    D. Control Unit

24. Which instruction type uses data memory?
    A. R-type
    B. Branch
    C. Load/Store
    D. Jump

In **MIPS architecture**, **R-type instructions** are encoded using a 32-bit format consisting of the following fields: opcode (6 bits, always 0 for R-type), rs (5 bits, first source register), rt (5 bits, second source register), rd (5 bits, destination register), shamt (5 bits, shift amount, assume 0 for sub), and funct (6 bits, determines the operation). The register mapping is given as follows: $s0 = 16, $t2 = 10, and $t4 = 12. The function code for the sub instruction is 34. Given the MIPS instruction **sub $t2, $s0, $t4**, construct the complete **32-bit machine code in binary**, and finally convert the result into **hexadecimal format**. 00000010000011000101000000100010 0x020C5022	

Best Wishes

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