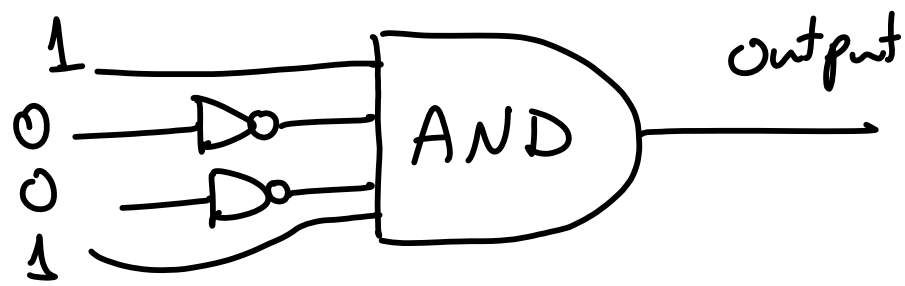
AGENDA

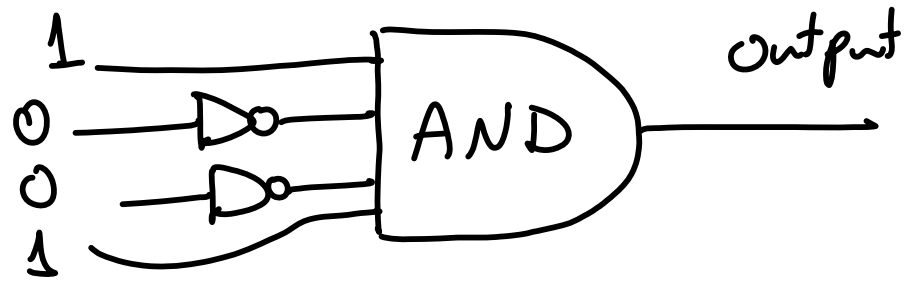
- Decoder

Decoder

Decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicate the presence of that code by a specified output

- Suppose you need to determine when a binary 1001 occurs on the inputs of a digital circuit
  - ↳ Output = 1 iff the first bit is 1
    and second bit is 0
    and third bit is 0
    and fourth bit is 1

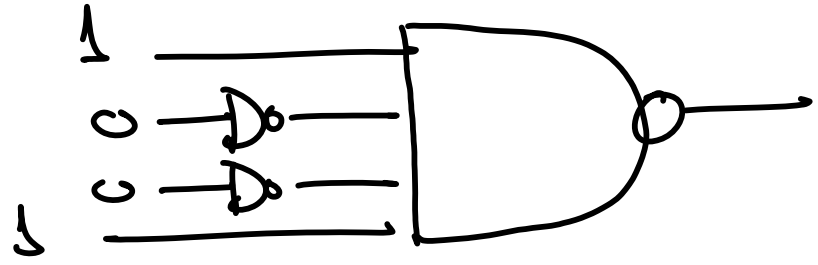




Decoding logic for the binary code 1001 with an active-high output

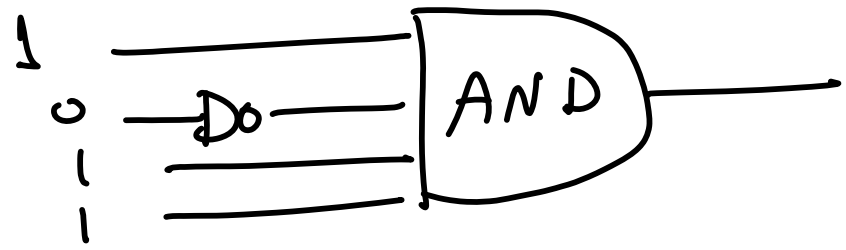
→ You should verify that the output is zero except when $A_0 = 1$, $A_1 = 0$, $A_2 = 0$ and $A_3 = 1$

- if a NAND is used in place of the AND gate, a low output will indicate the presence of the proper binary code



Ex Determine the logic required to decode the binary number 1011 by producing a HIGH level on the output

Sol



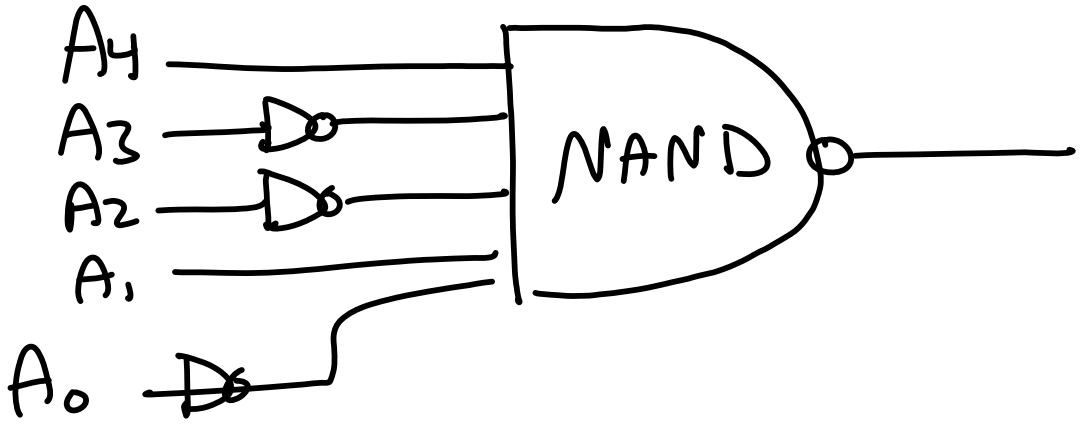
Ex Develop the logic required to detect the binary code 10010 and produce an active-low output

1	0	0	1	0

$$f = \overline{A}_4 + A_3 + A_2 + \overline{A}_1 + A_0$$

$$f = \overline{\overline{A}_4 + A_3 + A_2 + \overline{A}_1 + A_0}$$

$$f = \overline{A_4 \bar{A}_3 \bar{A}_2 A_1 \bar{A}_0}$$



Note

- Elevator example : lighting up one button on panel

- A decoder is a combinational circuit that converts binary information from n binary inputs to a maximum of 2^n unique output lines.

2x4 decoder

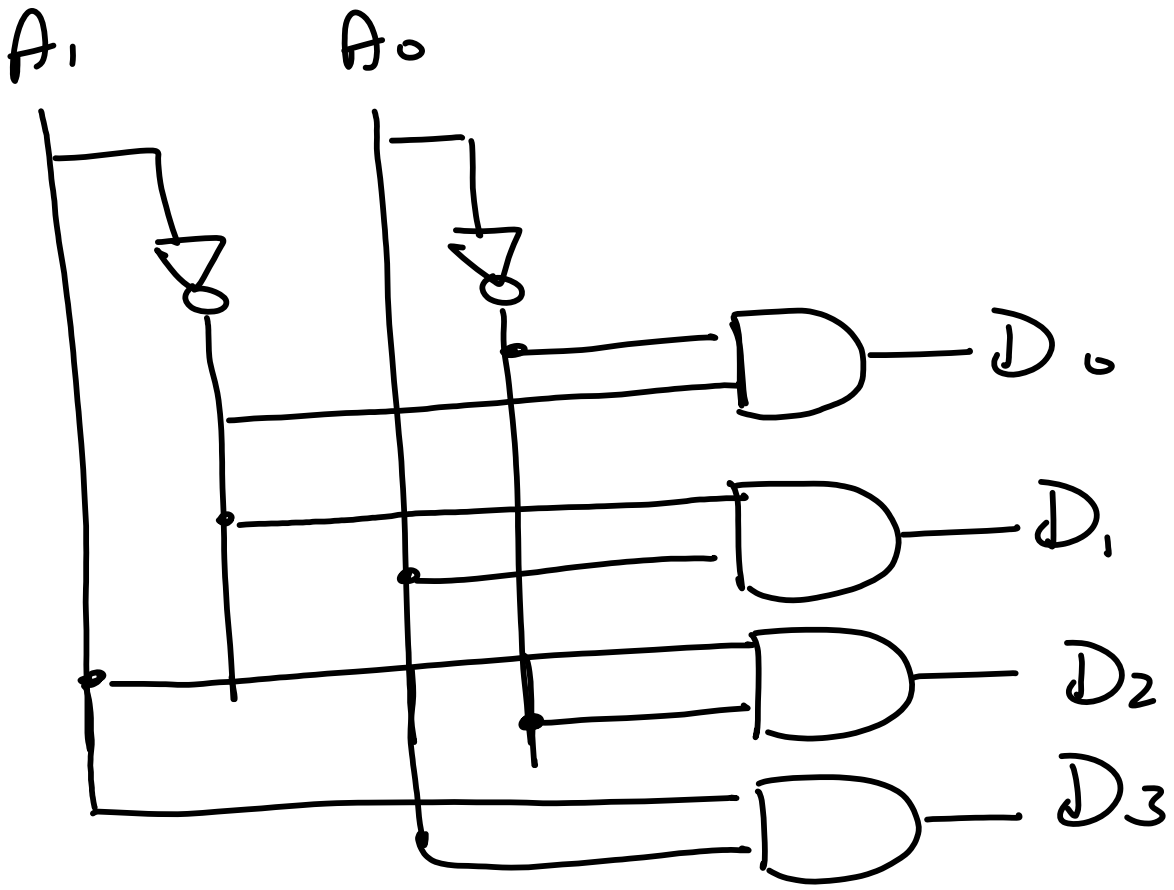
A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$D_0 = \overline{A_1}\,\overline{A_0}$

$D_1 = \overline{A_1}\,A_0$

$D_2 = A_1\,\overline{A_0}$

$D_3 = A_1 A_0$



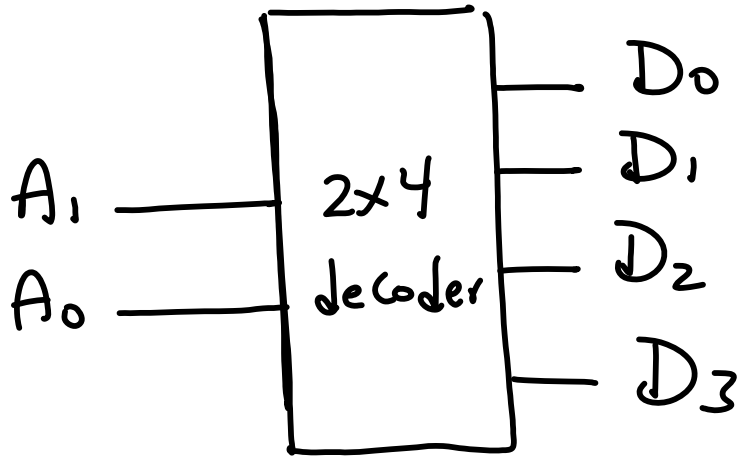
InfoNote

An instruction tells the processor what operation to perform.

instructions are in machine code (1s and 0s) and, in order for the processor to carry out an instruction, the instruction must be decoded.

Instruction decoding is one of the steps in instruction pipelining, which are as follows:

1. Instruction is read from the memory (Instruction fetch),
2. Instruction is decoded, operand (s) is (are) read from memory (operand fetch)
3. Instruction is executed, and the result is written back to memory



3x8 decoder

A_2	A_1	A_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$D_0 = \overline{A_2}\,\overline{A_1}\,\overline{A_0}$

$D_1 = \overline{A_2}\,\overline{A_1}\,A_0$

$D_2 = \overline{A_2}\,A_1\,\overline{A_0}$

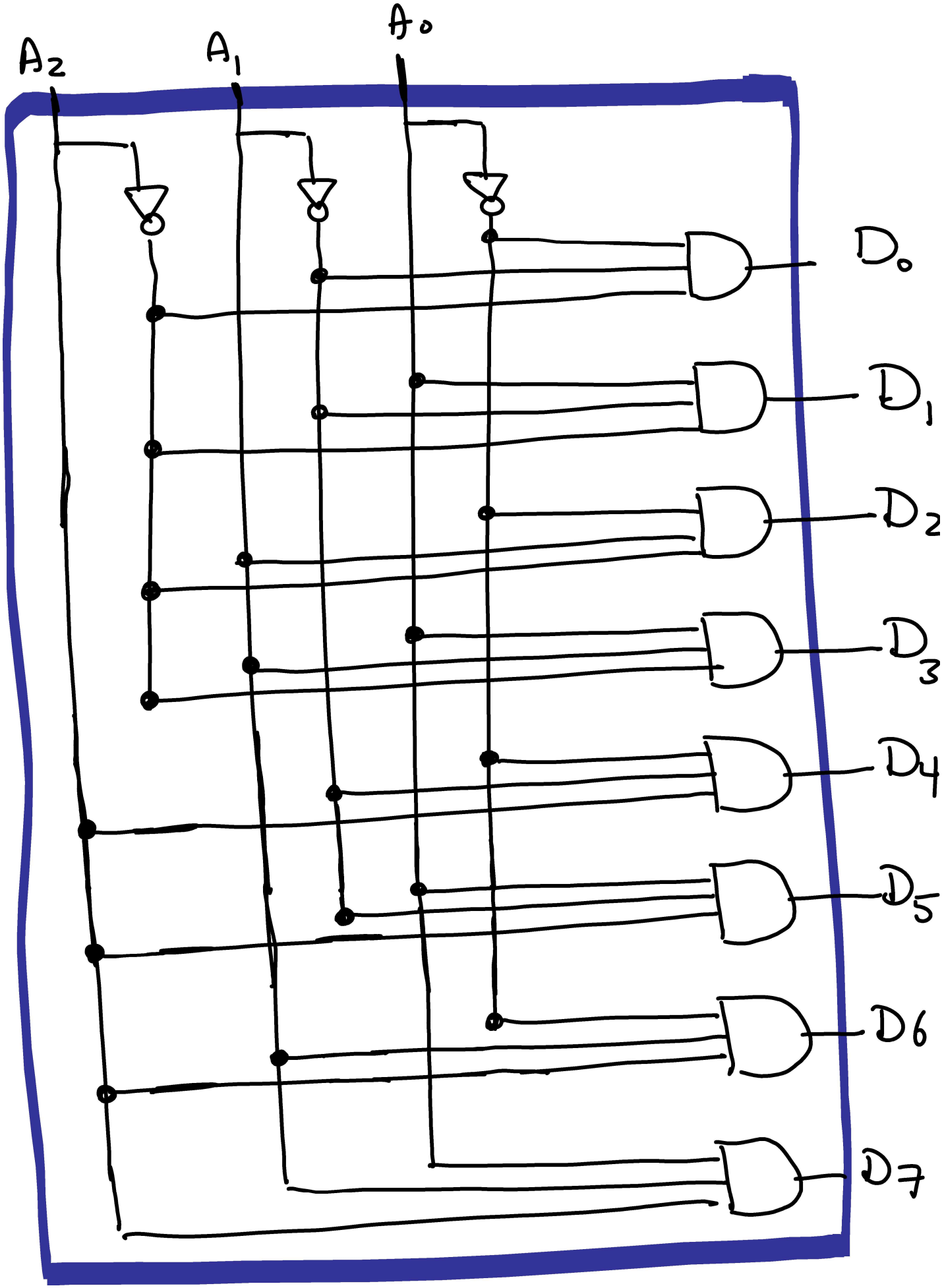
$D_3 = \overline{A_2}\,A_1\,A_0$

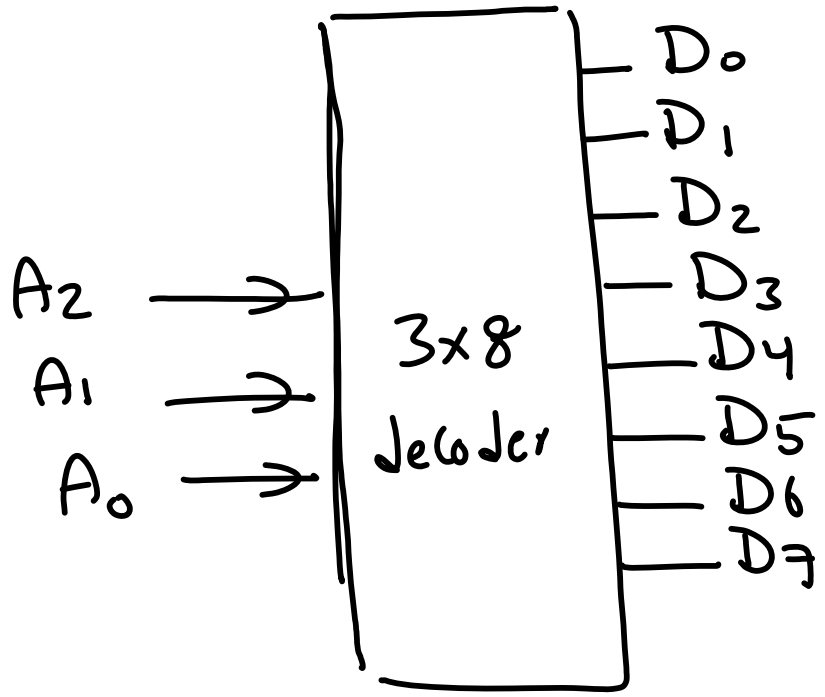
$D_4 = A_2\,\overline{A_1}\,\overline{A_0}$

$D_5 = A_2\,\overline{A_1}\,A_0$

$D_6 = A_2\,A_1\,\overline{A_0}$

$D_7 = A_2\,A_1\,A_0$


A2
A1
A0
D0
D1
D2
D3
D4
D5
D6
D7



When output D_0 is chosen?

if $A_2 A_1 A_0 = 000$

↳ $\overline{A_2}\,\overline{A_1}\,\overline{A_0}$

When output D_4 is chosen?

if $A_2 A_1 A_0 = 100$

↳ $A_2\,\overline{A_1}\,\overline{A_0}$

Prob

In order to decode all possible combination of four bits, sixteen decoding gates are required ($2^4 = 16$) — Design 4x16 decoder

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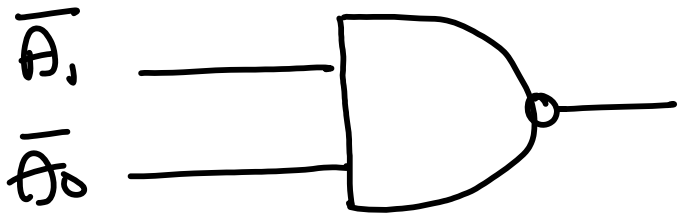
Ex

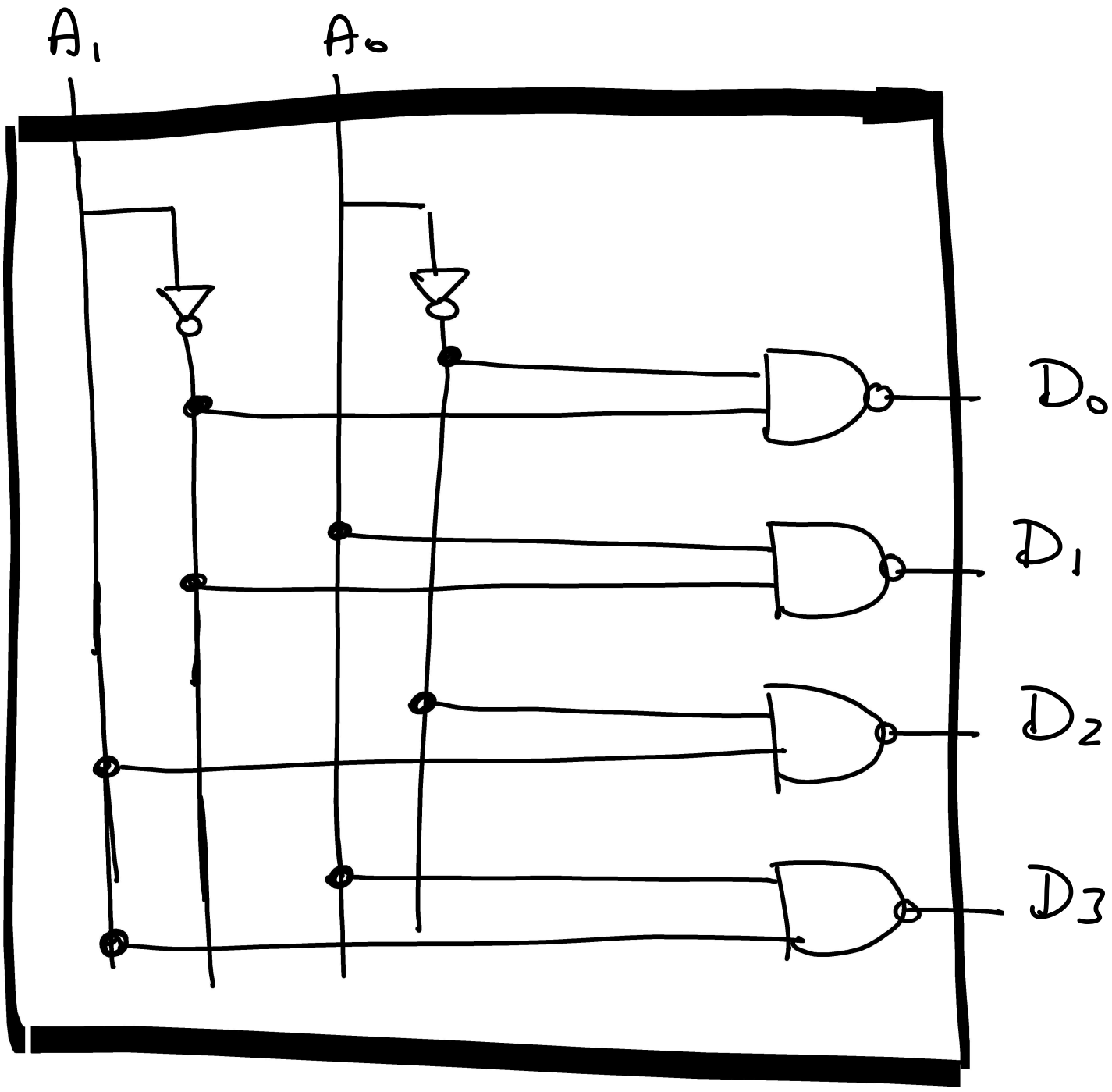
Design a 2x4 decoder with active-low output

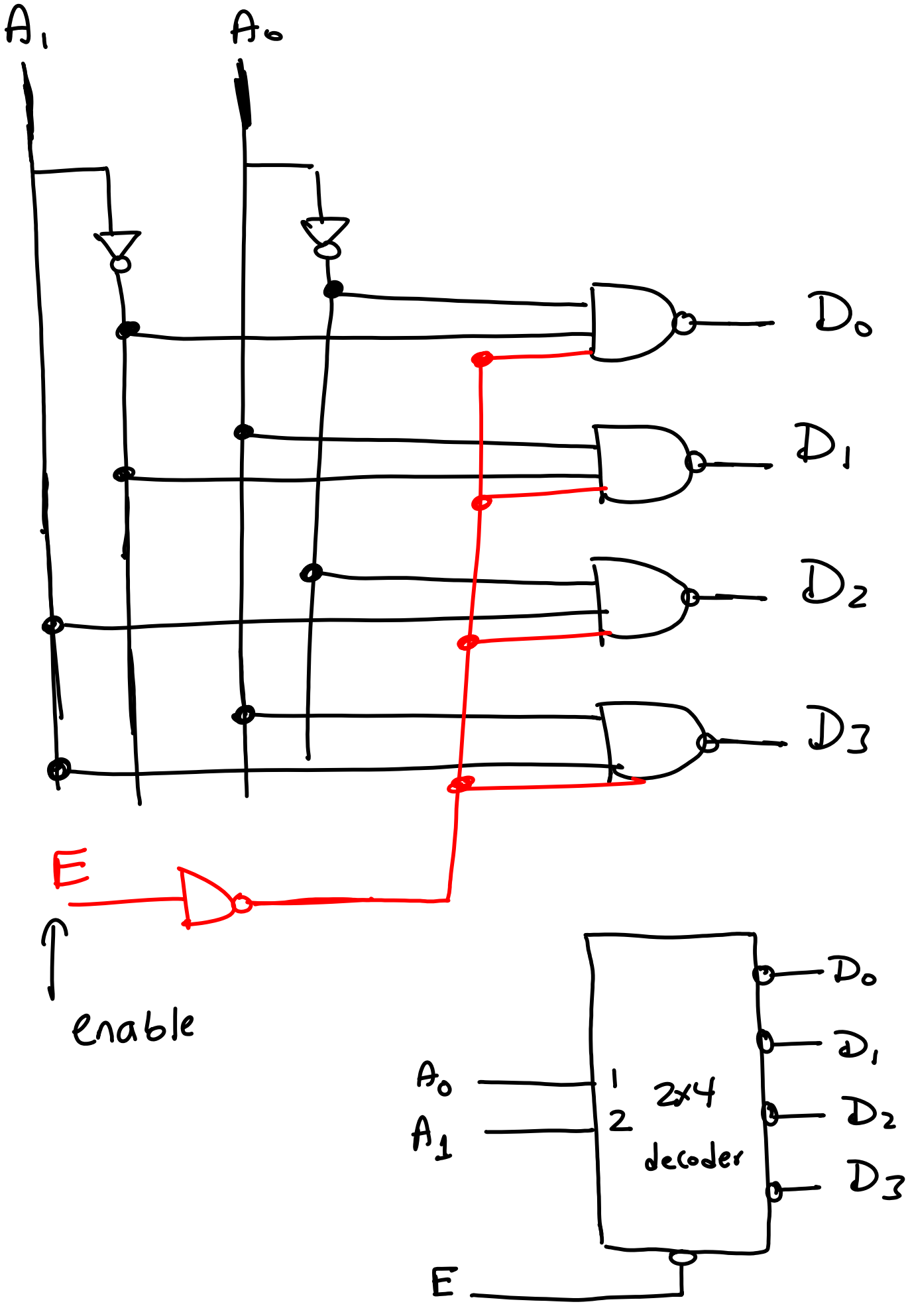
A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

$$D_0 = A_1 + A_0 = \overline{\overline{A_1 + A_0}}$$

$$\overline{D_0} = \overline{A_1}\,\overline{A_0}$$

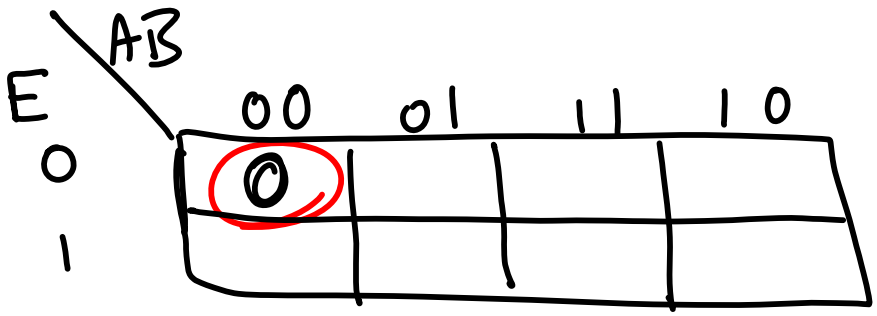



A1
A0
D0
D1
D2
D3

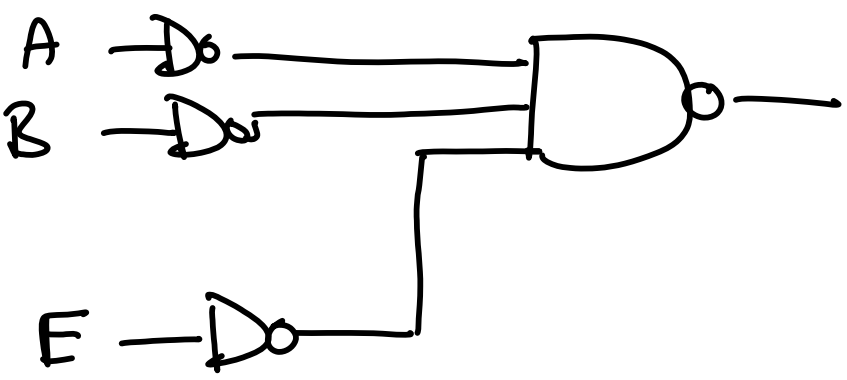

A1
A0
D0
D1
D2
D3
E
enable
A0
A1
1
2
2x4
decoder
D0
D1
D2
D3
E

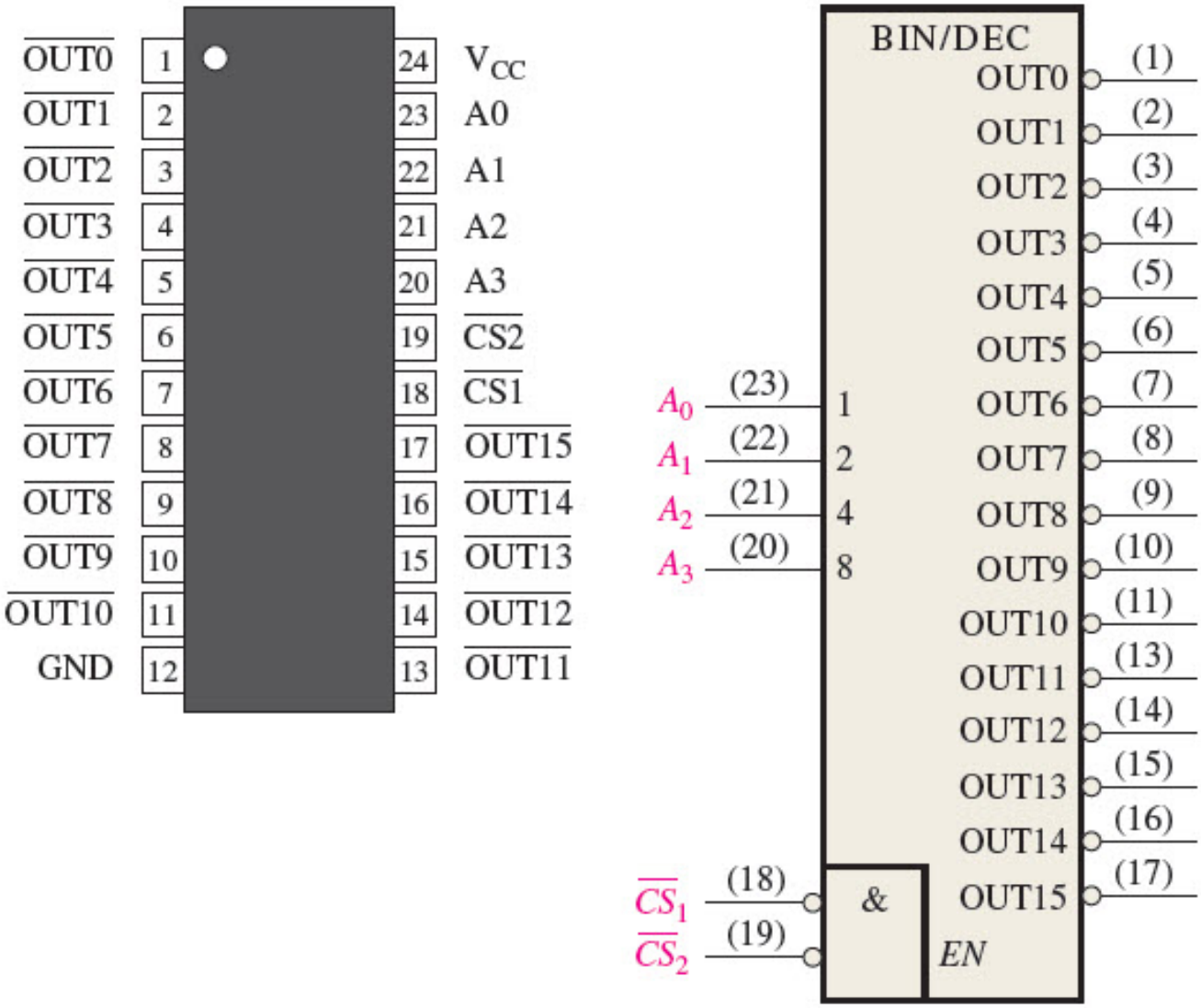
2x4 line decoder with enable

E	A	B	D_0	D_1	D_2	D_3
1	x	x	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0



$$\overline{D_0} = \overline{E}\,\overline{A}\,\overline{B}$$





(a) Pin diagram

(b) Logic symbol

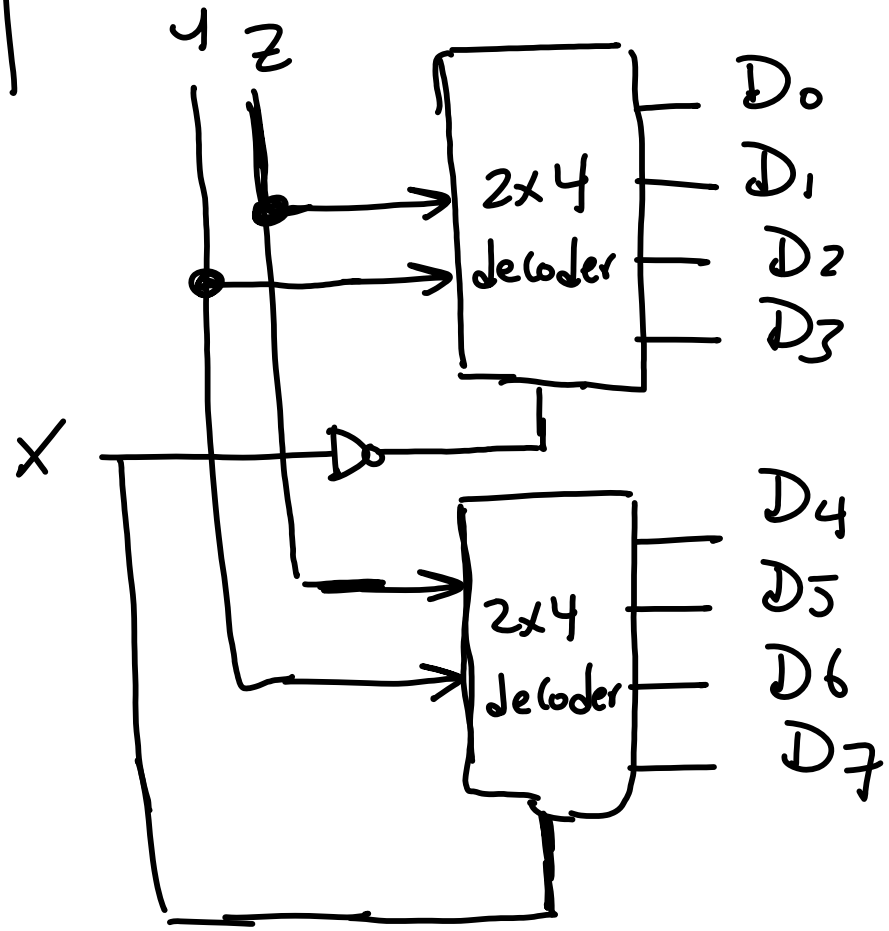
The 74HC154 1-of-16 decoder.

larger decoder

- Enable bit can be used for creating larger decoder

x	y	z
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

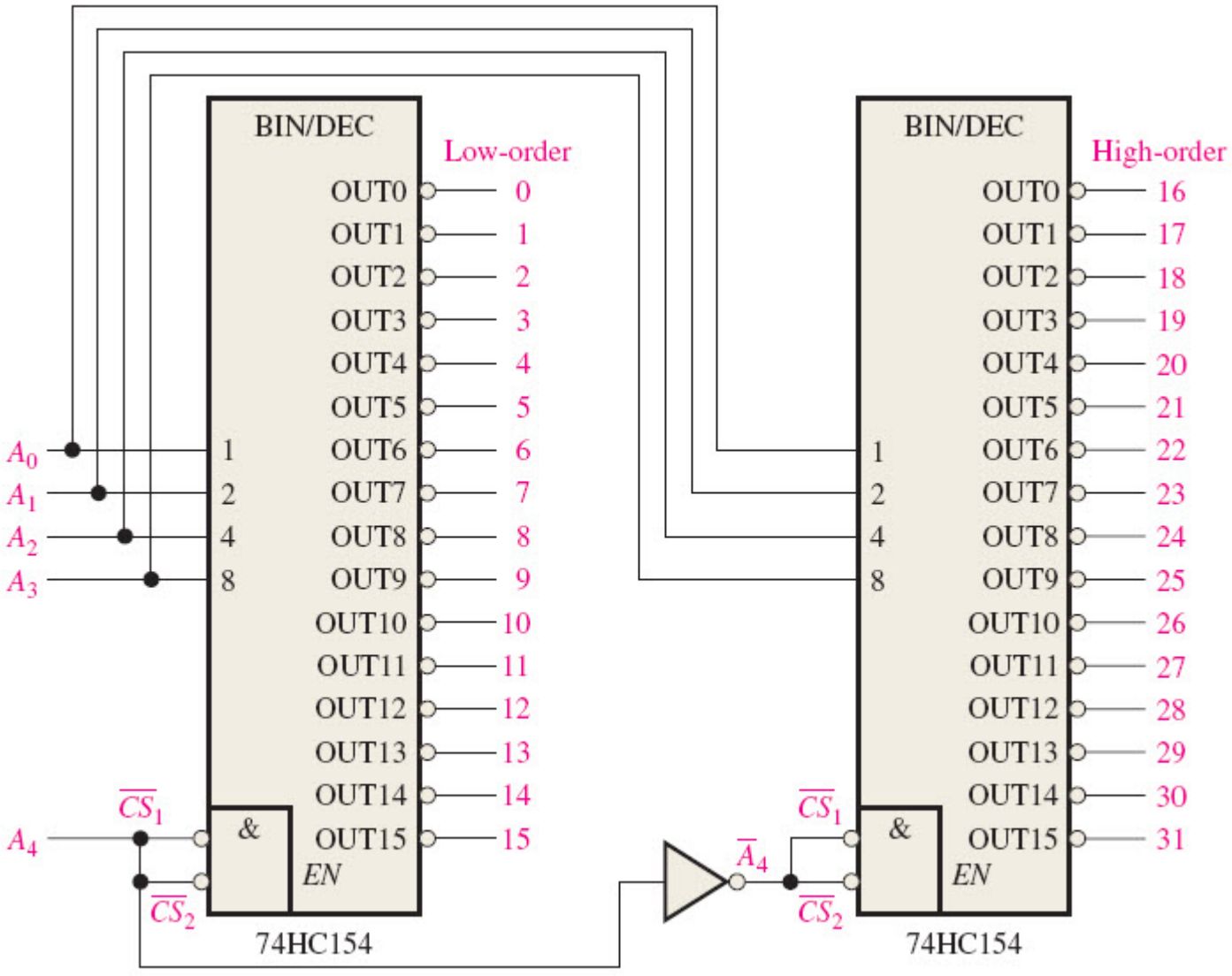
may be used as enable



Ex

A certain application requires that a 5-bit number be decoded. use 74HC154 decoders to implement the logic. the binary number is represented by the format

$A_4\ A_3\ A_2\ A_1\ A_0$

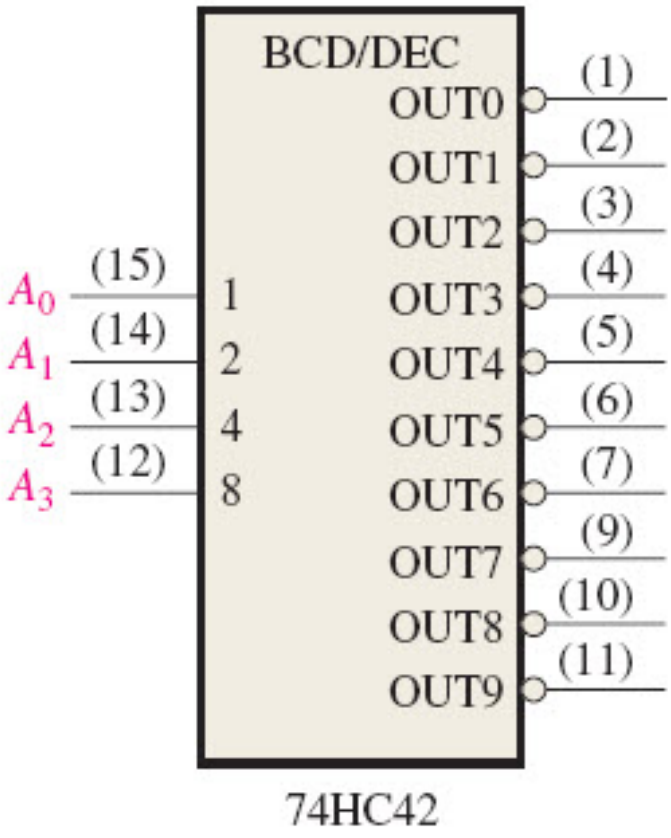


A 5-bit decoder using 74HC154s.

BCD-to-Decimal Decoder

Converts each BCD code into one of ten possible decimal digit

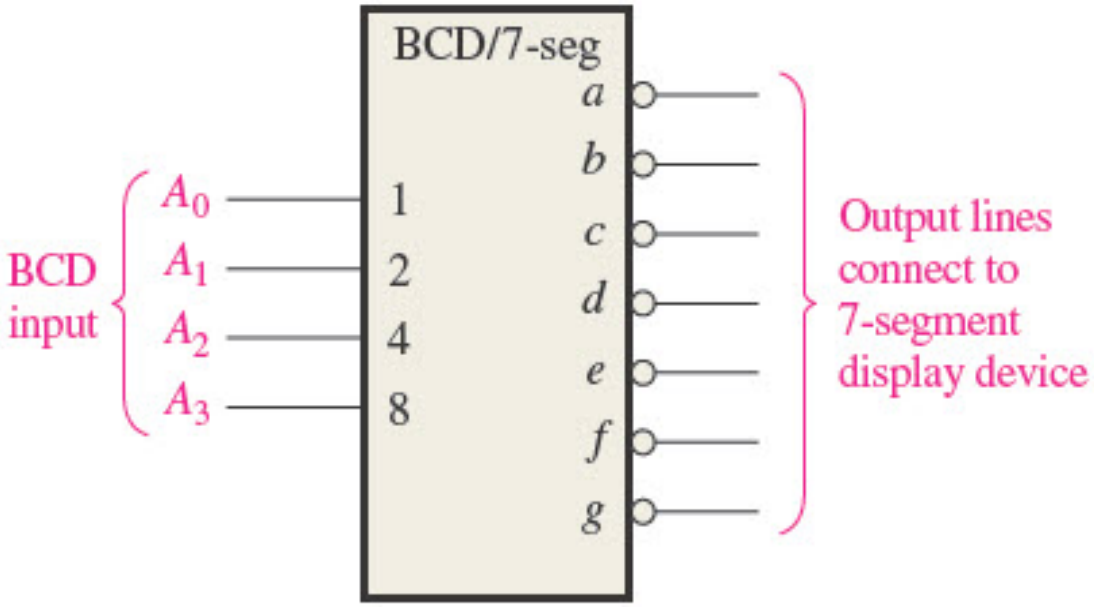
↳ 74HC42 ⇒ Four bits BCD inputs and ten active-low decimal outputs

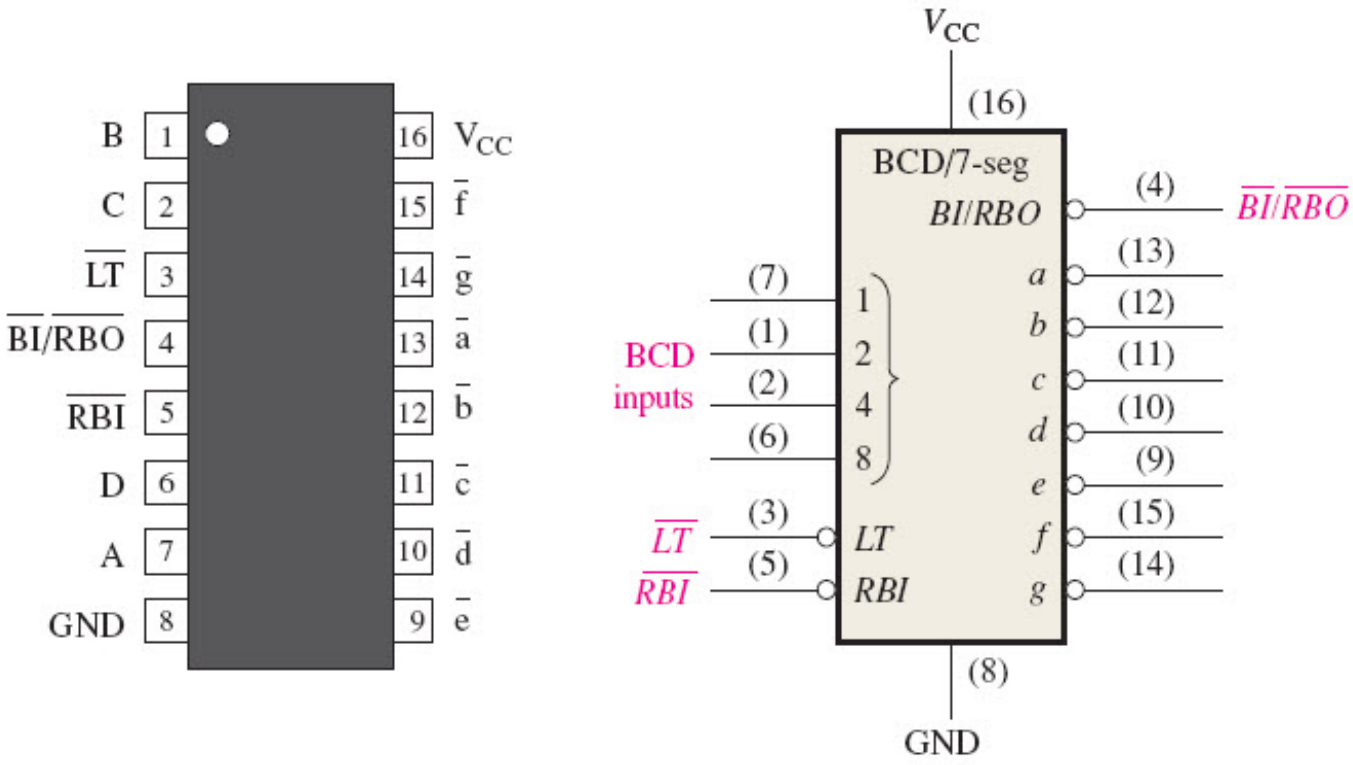


The 74HC42 BCD-to-decimal decoder.

BCD-to-7-Segment Decoder

BCD-to-7-segment decoder accepts the BCD code on its inputs and provides outputs to drive 7-segment display devices to produce a decimal readout





(a) Pin diagram (b) Logic symbol

The 74HC47 BCD-to-7-segment decoder/driver.

Report

Comment on $\overline{LT}$, $\overline{RBI}$, and $\overline{BI}/\overline{RBO}$

Note: A decoder with enable input can function as a Demultiplexer

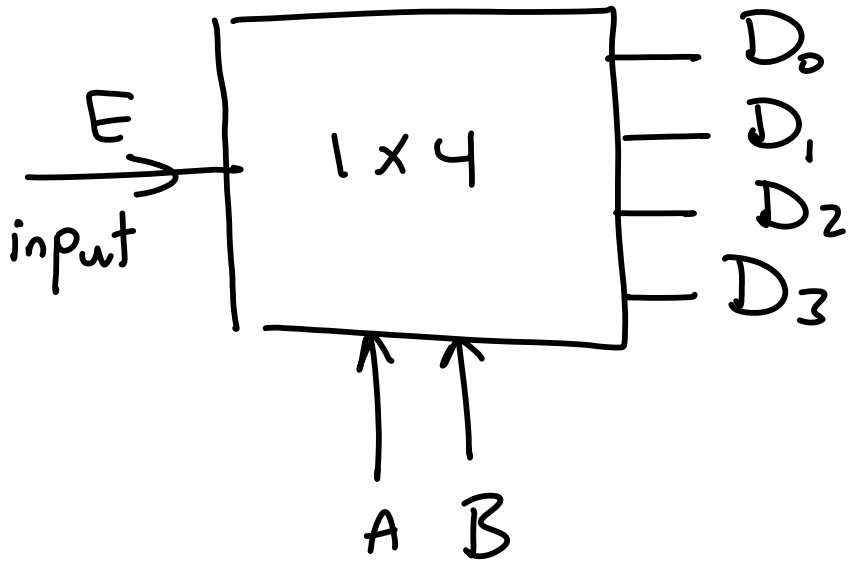
A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines

the selection of a specific output line is controlled by the bit values of n selection lines

E	A	B	D_0	D_1	D_2	D_3
1	x	x	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Look again

You can consider A, B as selection line, and enable as the data line



Note: Decoder can be used to implement a function

Ex Implement a full-adder circuit with a decoder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$\Rightarrow$ $S = \sum(1, 2, 4, 7)$

$C = \sum(3, 5, 6, 7)$