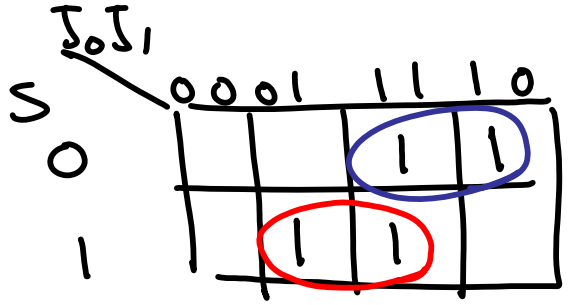
Ex

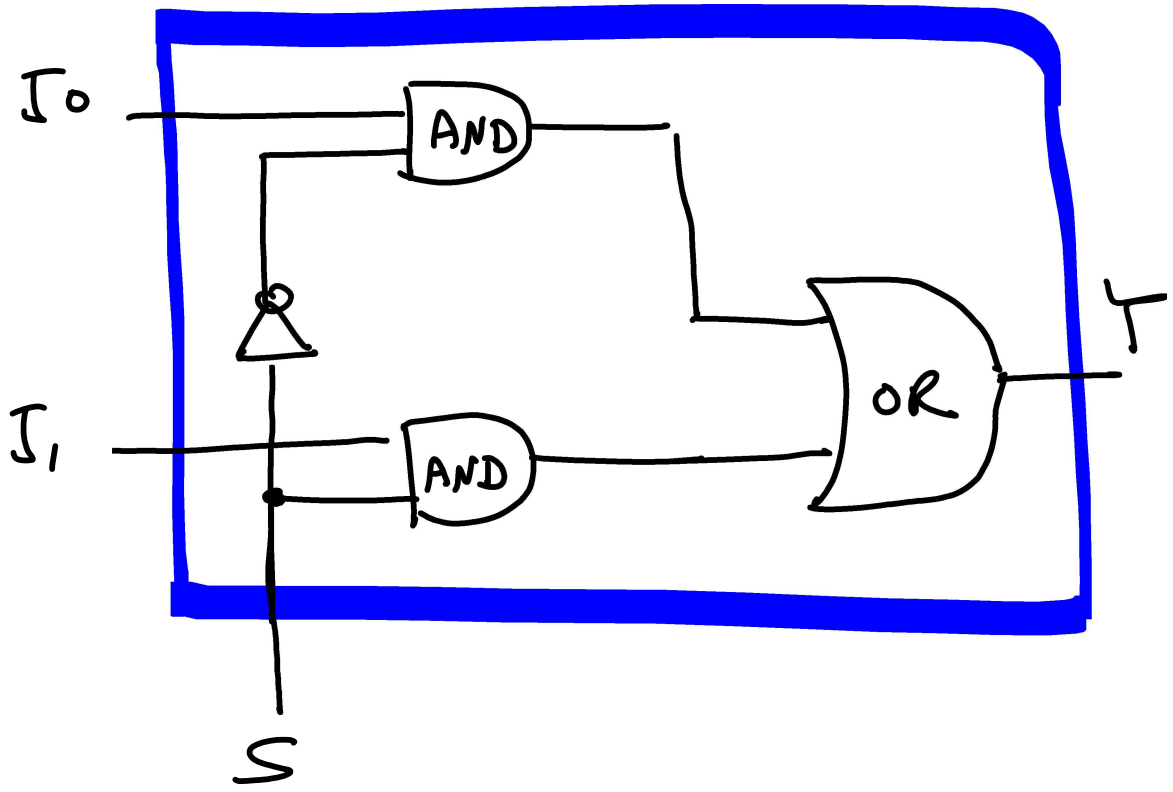
Design a digital circuit that can select between two 1-bit number I_0, I_1. the output should be $Y = I_0$ when $S = 0$, and $Y = I_1$ when $S = 1$

$$Y = \begin{cases} I_0 & S = 0 \\ I_1 & S = 1 \end{cases}$$

S	I_0	I_1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

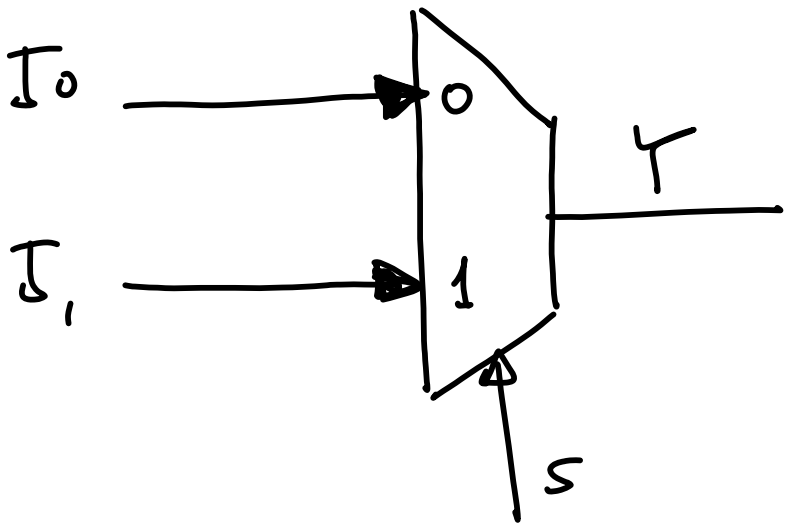


$$Y = \overline{S} I_0 + S I_1$$



this Circuit is called Multiplexer

2 x 1 Multiplexer



2x1 Mux

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination

Inputs: 2^n input lines

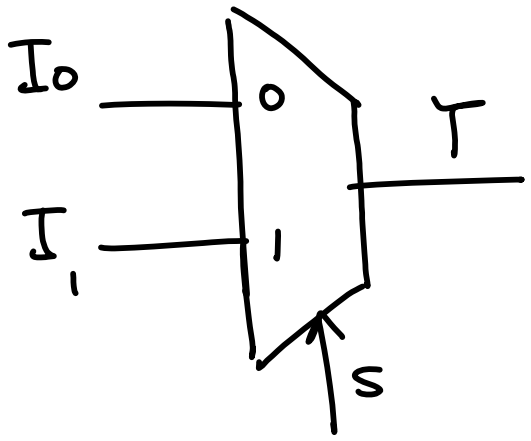
n selection bits

Output: 1 output line

Ex 2 x 1 MUX

we can use function table

S	Y
0	I_0
1	I_1



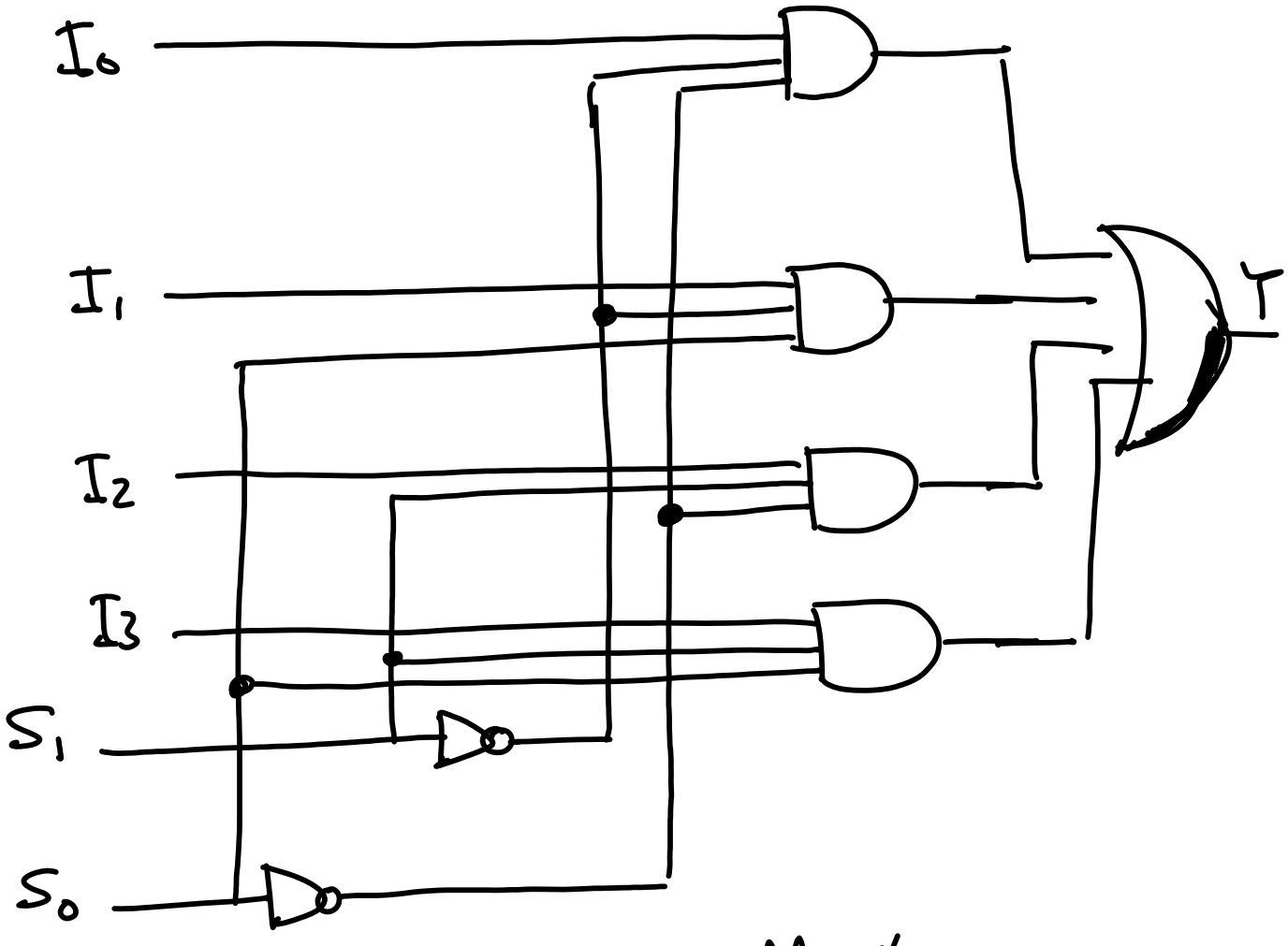
$\rightarrow Y = \bar{S} I_0 + S I_1$

Ex

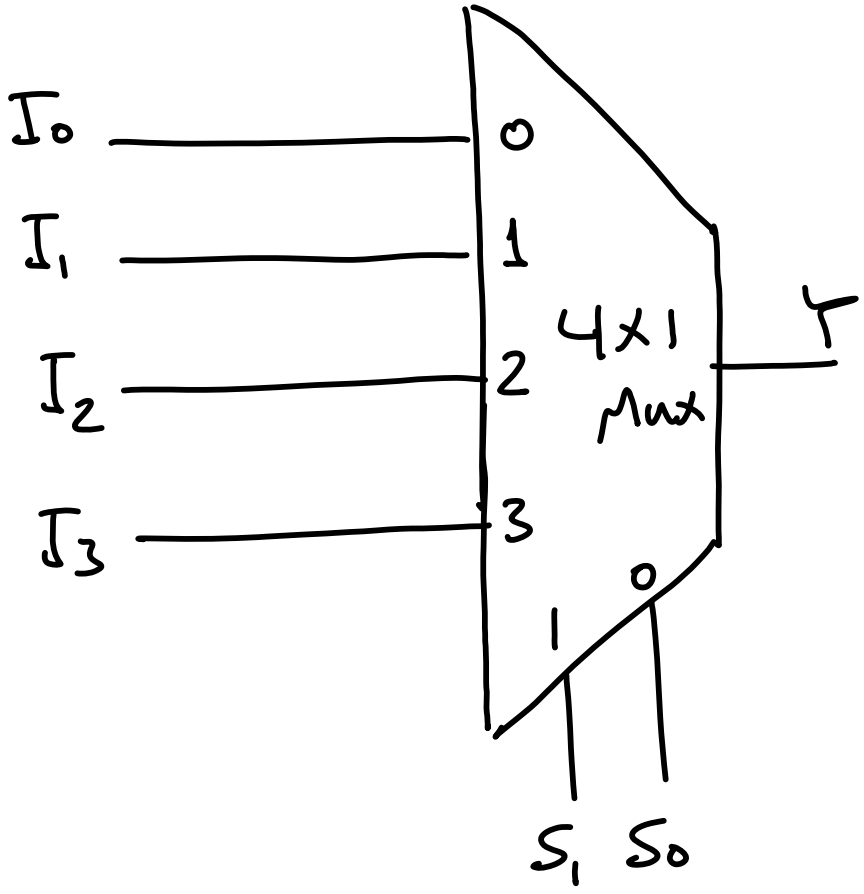
4 x 1 Mux

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$\Rightarrow Y = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$



4 x 1 Mux



InfoNote

A bus is a multiple conductor pathway along which electrical signals are sent from one part of a computer to another.

In a computer networks, a shared bus is one that is connected to all the microprocessors inthe system in order to exchange data

A shared bus may contain memory and input/output devices that can be accessed by all the microprocessors in the system. Access to the shared bus is controlled by a bus arbiter that allows only one microprocessor at a time to use the system's shared bus.

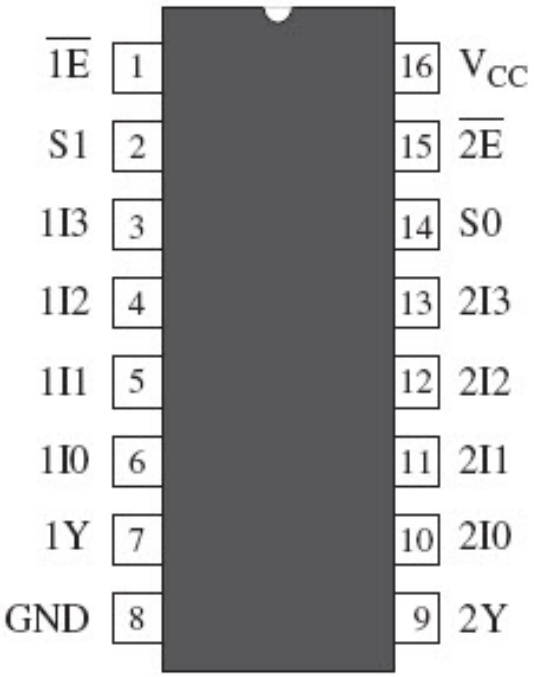
Note

Multiplexer ≡ Data Selector

74HC153 ⇒ dual four-input data selector/multiplexer

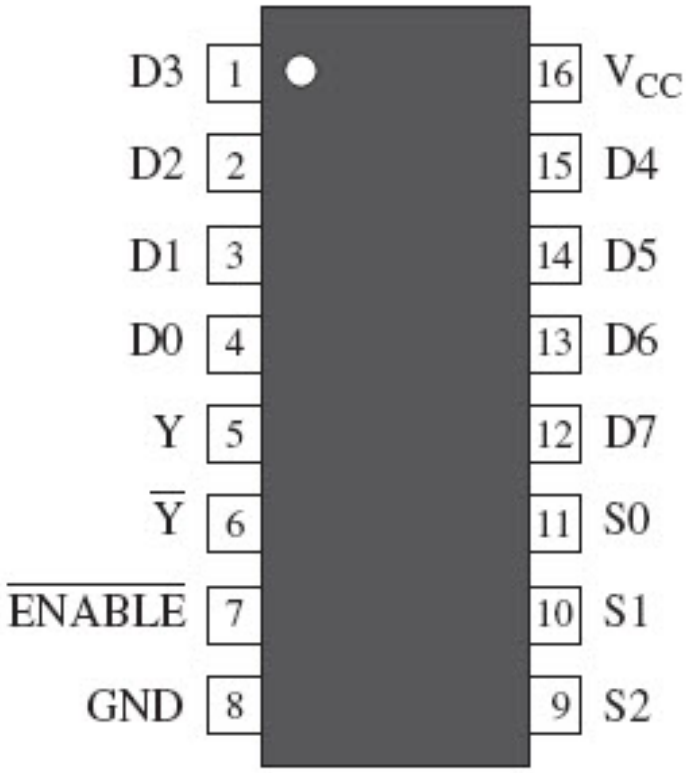
- the inputs to one of the multiplexers are 1I0 through 1I3
- the inputs to the second multiplexer are 2I0 through 2I3

- the data select inputs are S0 and S1 and the active-low enable inputs are 1E and 2E — each of the multiplexers has an active-low enable input



The 74HC153 dual four-input data selector/multiplexer.

74HC151 : 8x1 Mux

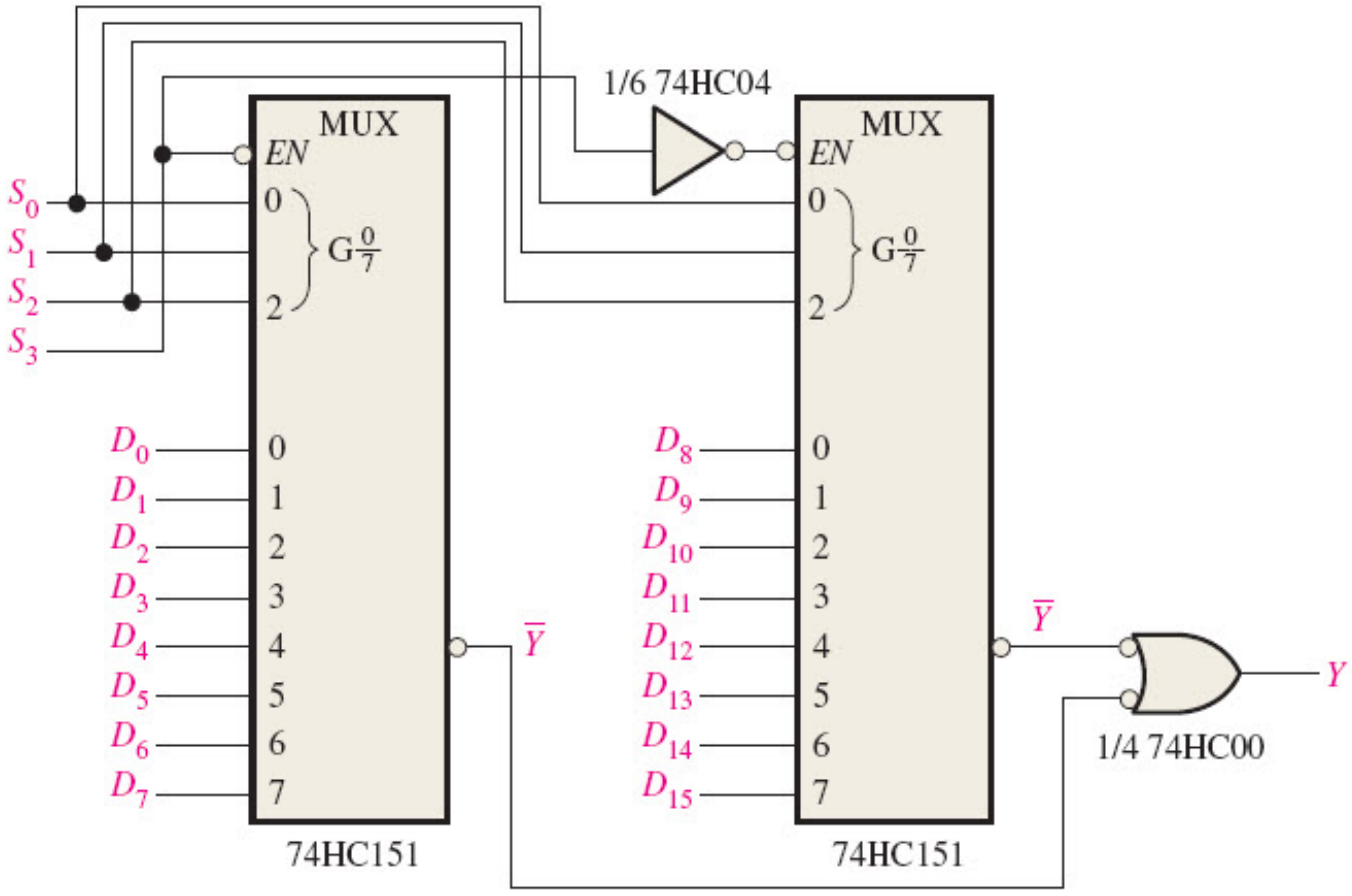


The 74HC151 eight-input data selector/multiplexer.

Notice that the data output and its complement are both available

Report :

use 74HC151s and any other logic necessary to multiplex 16 data lines onto a single data_output line.



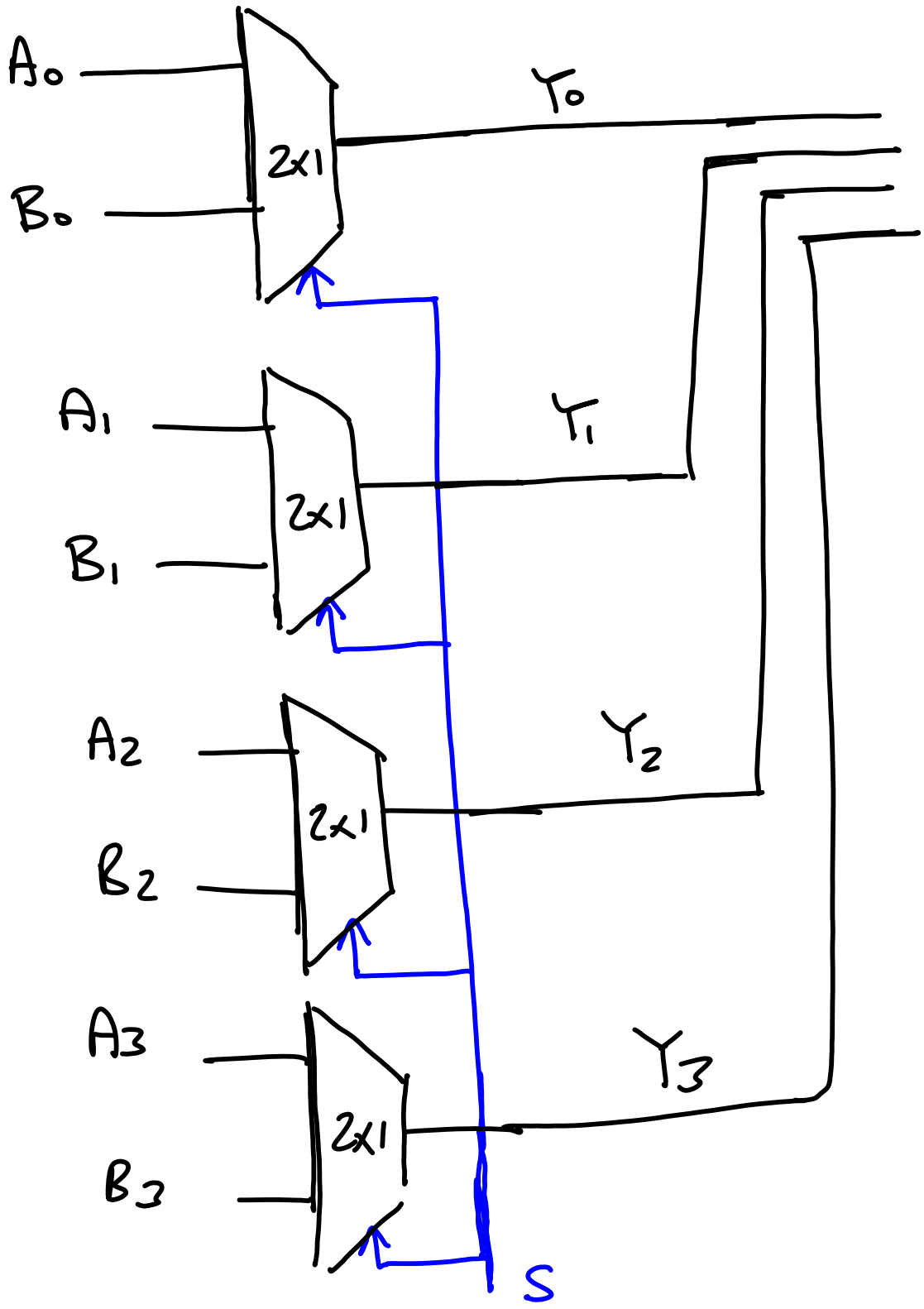
A 16-input multiplexer.

Prob :

Determine the codes on the select inputs required to select each of the following data inputs : D_0, D_4, D_8, D_{13}

Ex choose one of two 4-bit numbers

Sol Quadrable 2x1 Mux



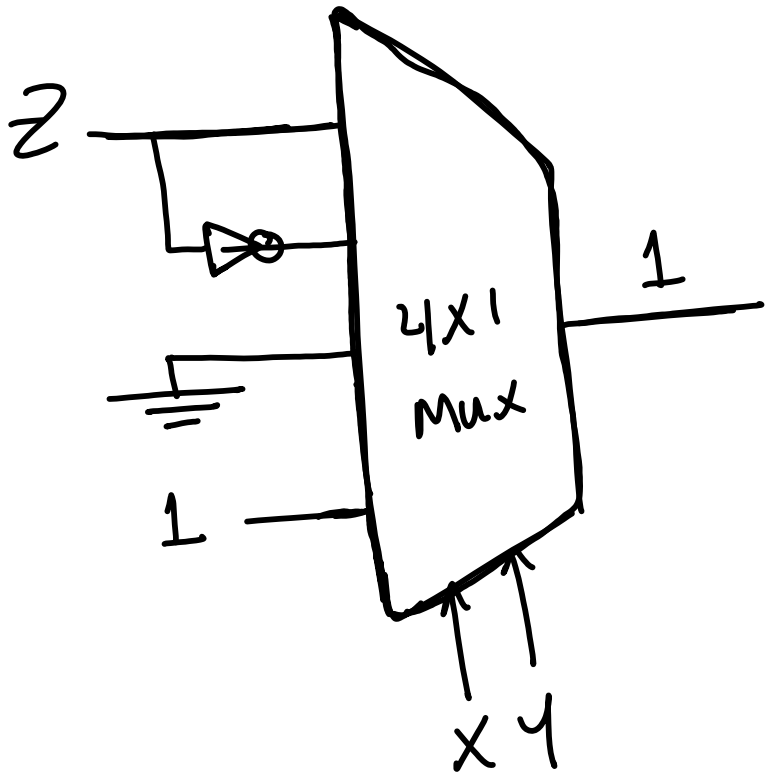
Function implementation with MUX

- function with n variables has 2^n truth table entries
  - wire up 1 and 0 to each input of 2^n-to-1 line MUX
- can be done more efficiently
  - 2^{n-1} to 1 MUX sufficient
- Idea
  - wire up n-1 variables to selection bits
  - function might depend on nth variable
    - use for 2^{n-1} inputs

Ex implement the Boolean function F represented in the truth table below

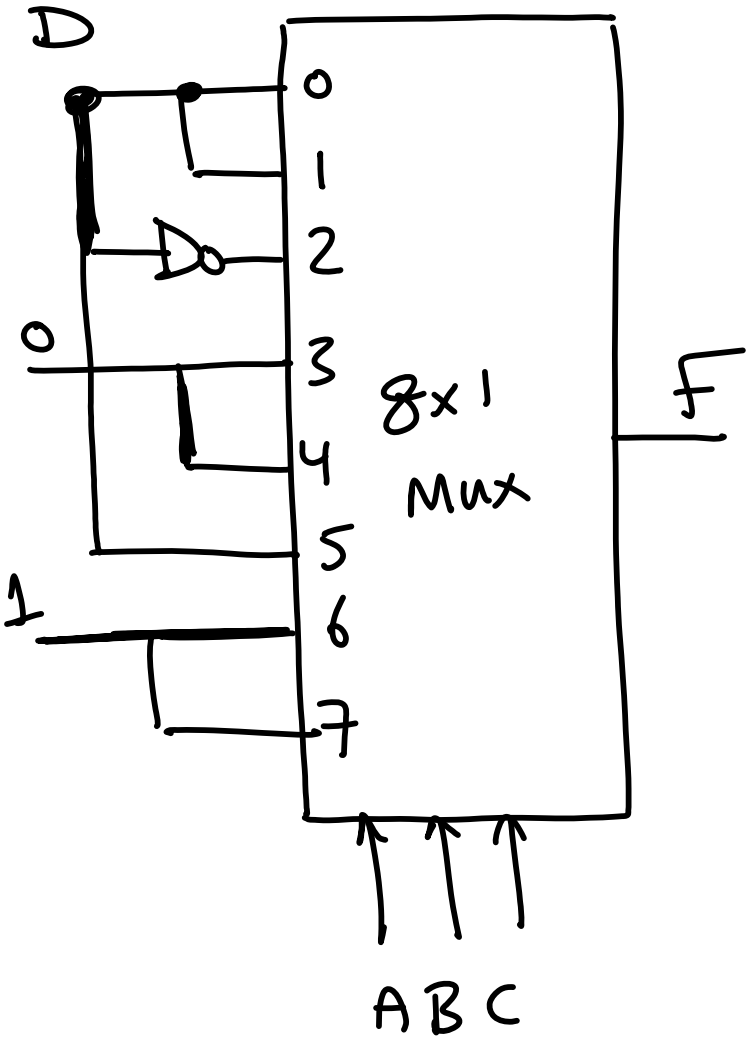
X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

What is the relation between F and Z



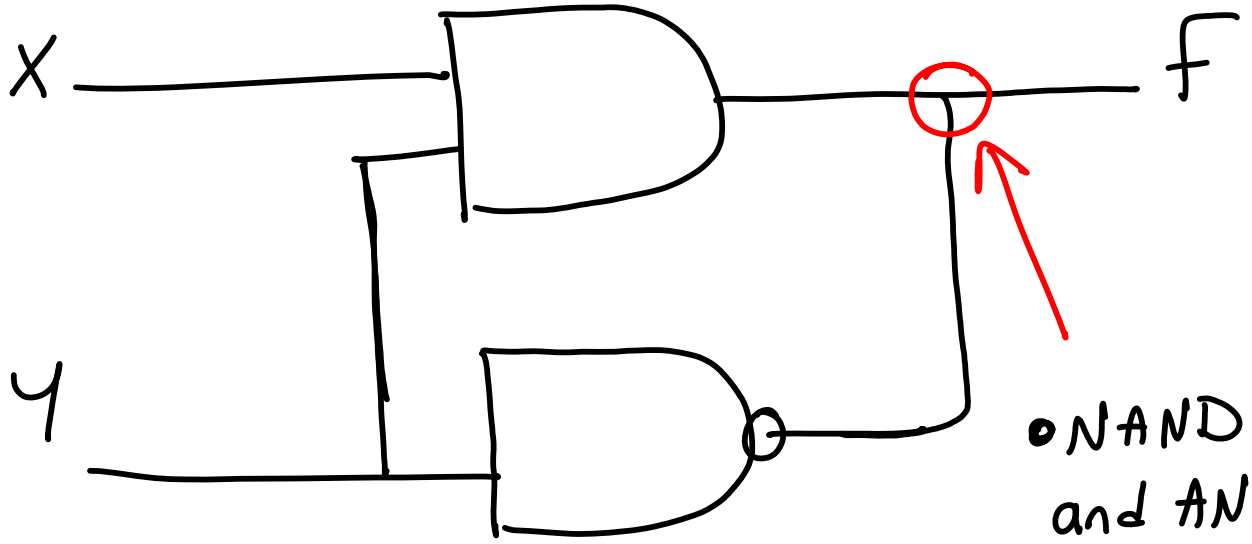
Ex

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



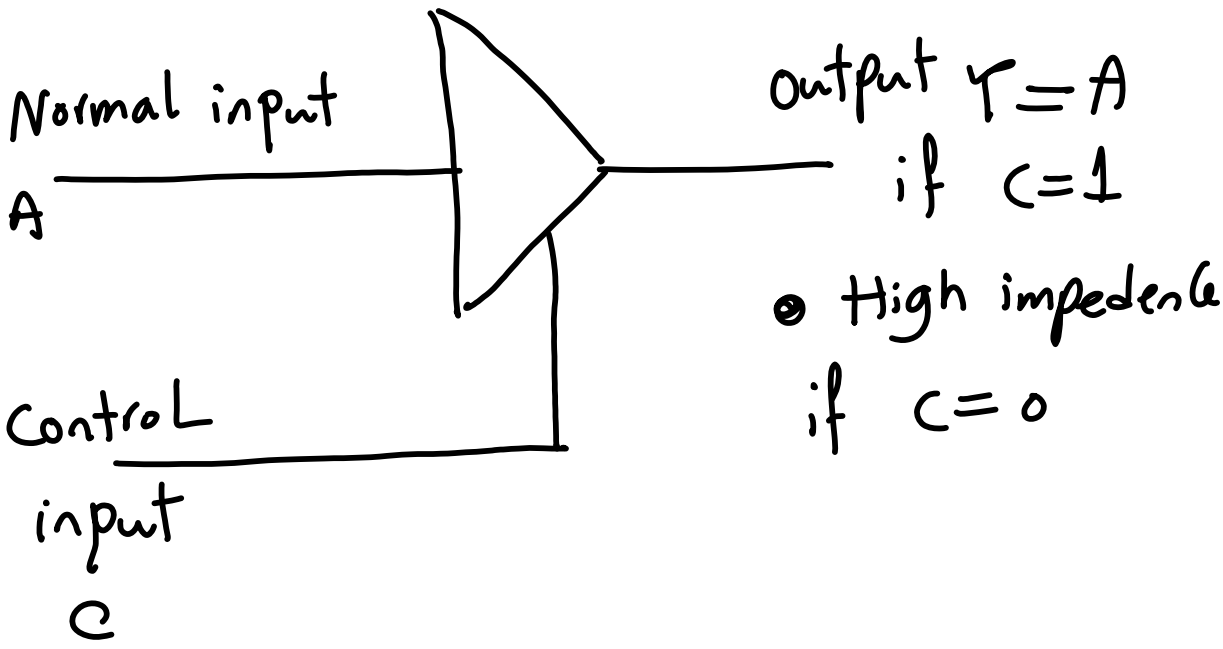
Three – state Gate

Did you see this Circuit before ?



- NAND and AND will try to drive output

- Sometimes necessary to disconnect a gate
- three state
  - 0 or 1 Boolean value
  - High impedence



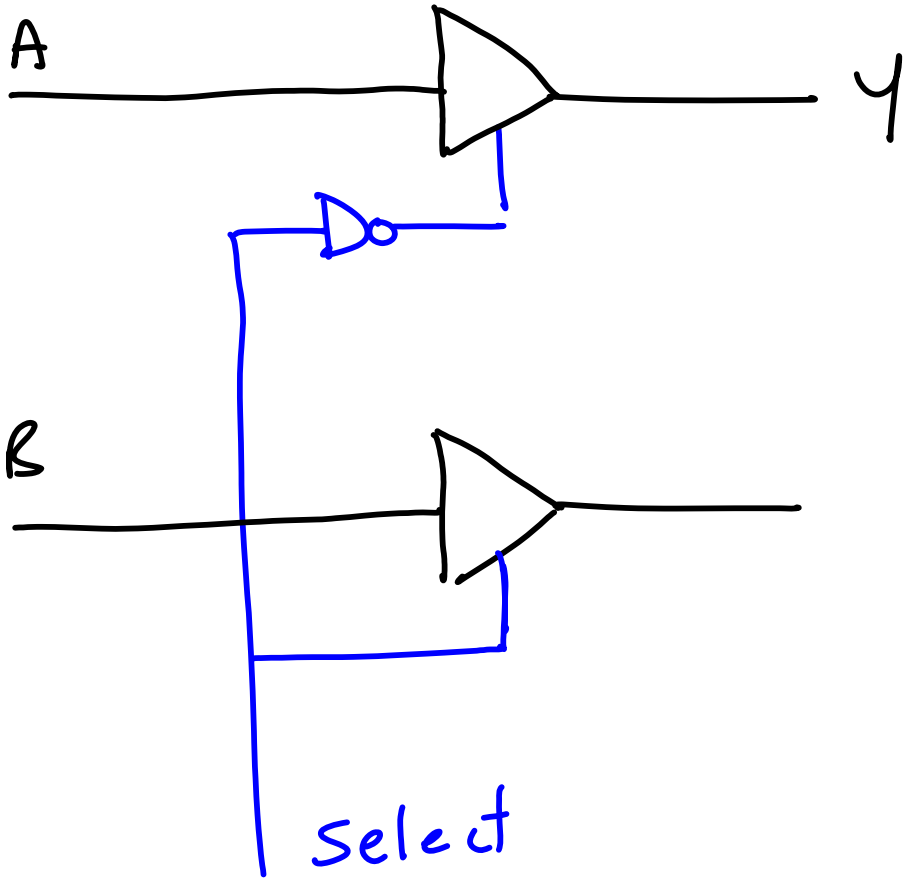
- High impedence acts as if gate is disconnected
- A different type of logic gate
  - Instead of two states (0, 1), it exhibits three states (0, 1, Z)
- Z is called high impedence

- when in Z-state, the circuit behaves like an open circuit (the output behaves like an open circuit)

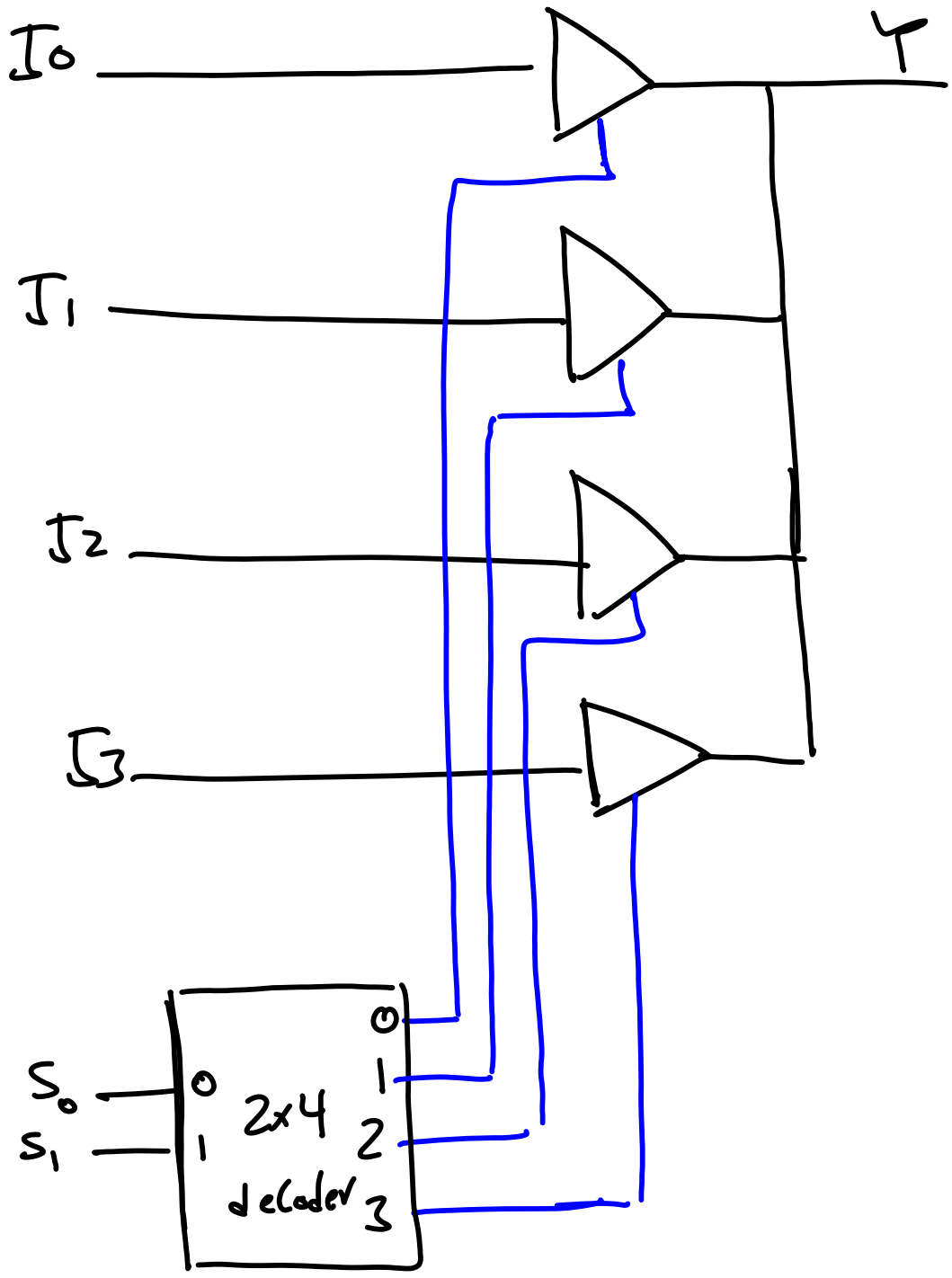
(the output appears to be disconnected,

and the circuit has no logic significance)

Multiplexer with three-State gate



2x1 MUX


I0
I1
I2
I3
Y
S0
S1
0
1
2x4
decoder
0
1
2
3