

Chapter 3

A Top-Level View of Computer Function And Interconnection – Part 03 Bus

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Bus

| Agenda

- 🌀 Intro
- 🌀 Bus Basics
- 🌀 Bus C/Cs
- 🌀 Parallel – Serial Transmission
- 🌀 Internal and External Buses
- 🌀 General Bus C/Cs
- 🌀 Bus Protocol
- 🌀 Handshaking
- 🌀 Synchronous and asynchronous
- 🌀 Single-Ended and Differential Bus

expansion
bus

| Intro...

- A bus allows two or more devices to communicate with each other, generally for the purpose of transmitting data.
- A bus is a set of physical wires and connectors and a set of electrical specifications.
- A bus can be either internal or external to a system.

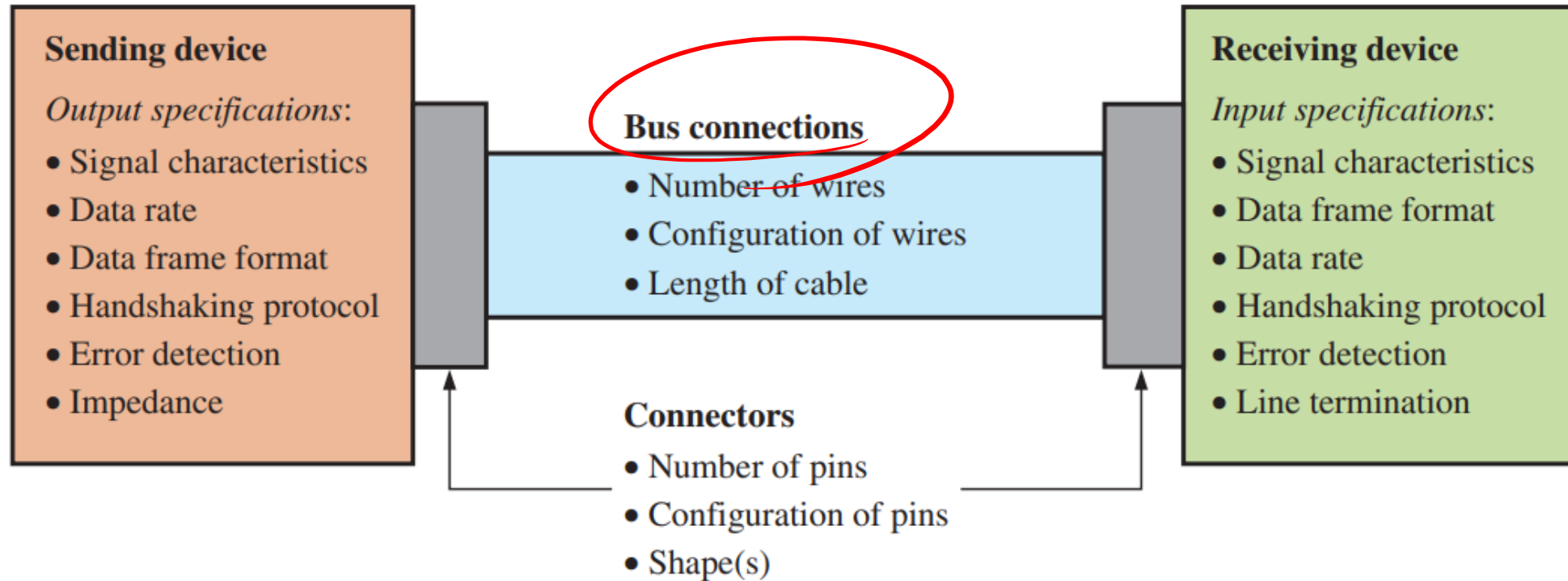
Conductor

↓ expansion

| Bus C/Cs

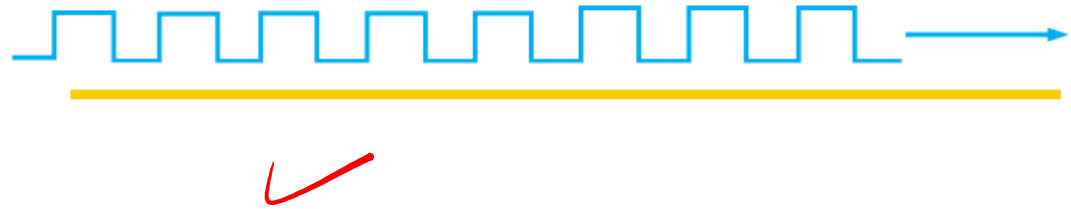
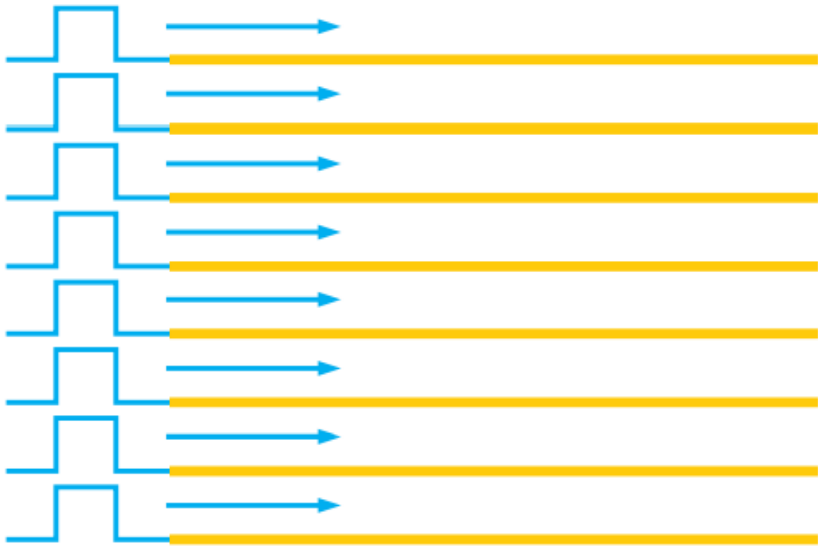
- The electrical properties of a typical bus include but are not limited to:
 - signal format, signal voltage levels, **clock frequency**, data transfer speed, **bandwidth**, data frame format, data rate, handshaking protocol, error detection, impedances, and line termination.
- Each device connected to a bus must be **compatible** with the bus specifications in order to communicate.
- A **sending** device can also be a **receiving** device, and a receiving device can also be a sending device

| Bus C/Cs



| Parallel – Serial Buses

- Buses can be either **parallel or serial**.
- A **parallel bus** carries data bits simultaneously, and a serial bus carries data bits sequentially one at a time



| Parallel – Serial Buses

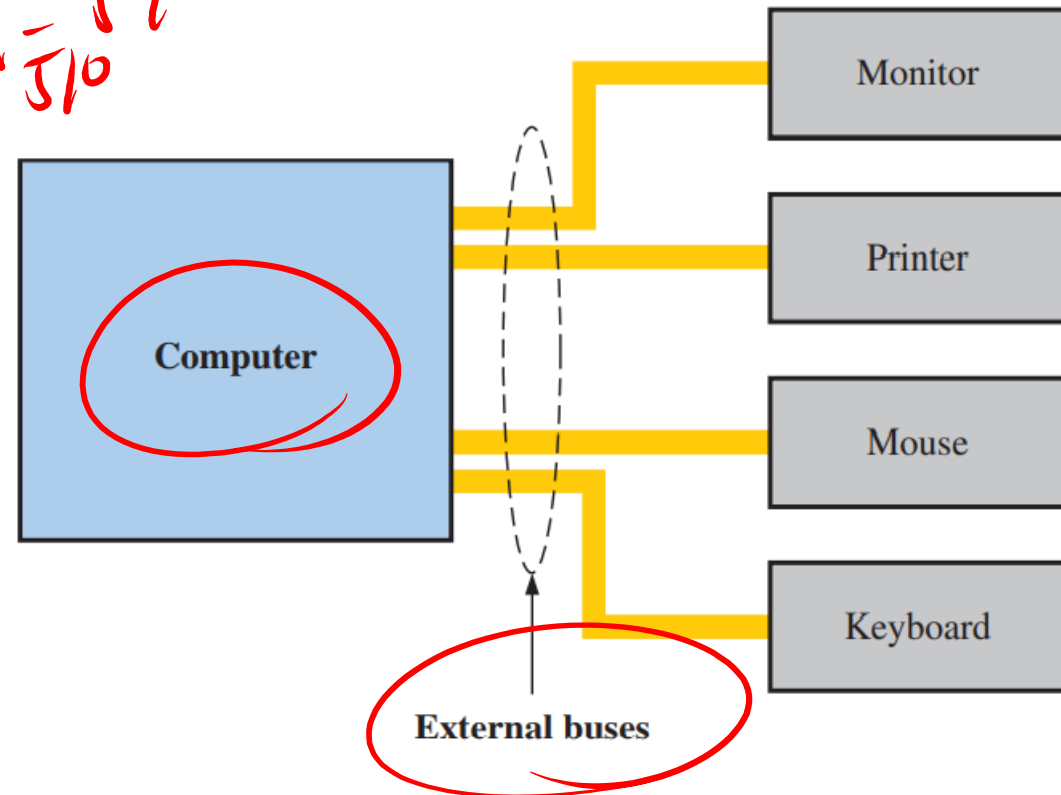
- It would seem that a parallel bus would transmit data faster than a serial bus because multiple data bits can be sent simultaneously. However, this is not always the case
- As data rates increase
 - **Crosstalk** across parallel bus lines,
 - Timing skew between bus lines, and
 - **EMI** (electromagnetic interference) become problems that limit the speed.
- Serial buses are not limited by those factors and can actually transmit data at higher rates than parallel buses in many situations

Parallel bus

| Internal and External Buses

- **Internal buses** carry information within a system,
- **External buses** (also known as expansion buses) are used to connect one system to another separate system.

*CPU - memory
memory - I/O
CPU - I/O*



| General Bus C/Cs

A bus is typically described by the following parameters:

- **Width:** The number of bits that a bus can transmit at one time.
 - The width of typical buses can vary from 1 bit for a serial bus up to 64 bits for a parallel bus.
- **Frequency:** The clock frequency at which a bus can operate
- **Transfer speed:** The number of bytes per clock cycle
- **Bandwidth:** The number of bytes per clock cycle times the number of clock cycles per second; that is, transfer speed times frequency. Bus bandwidth is sometimes called throughput.

| General Bus C/Cs

■ **Bus Bandwidth** =
$$\frac{\text{Width(bits)} \times \text{Frequency(MHz)}}{8 \text{ bits per byte}}$$

- A certain bus is specified with a width of 32-bits and a frequency of 66 MHz. Determine the bus bandwidth. Note that Bps is bytes per second

$$\underline{\text{Bandwidth}} = \left(\frac{32}{8} \right) * \underline{\underline{66 \text{ MHz}}} = \underline{\underline{264 \text{ MBps}}}$$

| General Bus C/Cs

- **Bus Bandwidth** = $\frac{\text{Width}(\text{bits}) \times \text{Frequency}(\text{MHz})}{8 \text{ bits per byte}}$
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| General Bus C/Cs

TABLE 13-1

Bus	Width (bits)	Frequency (MHz)	Transfer Speed (bytes/cycle)	Bandwidth (MBps)	
				Decimal	Binary
✓ ISA (16 bit)	16	8.3	2	16.6	15.9
✓ PCI	32	33	4	132	125.9
PCI-X	32	66	4	264	251.8
AGP	32	66	4	264	251.8

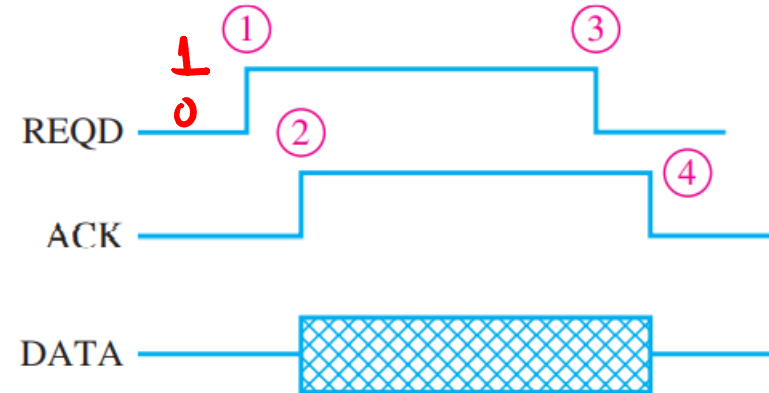
| Bus Protocol

- **Bus protocol** is a **set of rules** that allow two or more devices to communicate through a bus.
- Buses provide for **data transfer, address selection, and control.**
- **Each device** connected to a bus has an address assigned to it for identification and command signals as well as control signals to implement the protocol.
- These signals allow the devices to work properly together by identifying each other and communicating back and forth. One device can **send a request** to another device and get an **acknowledgement or reply**

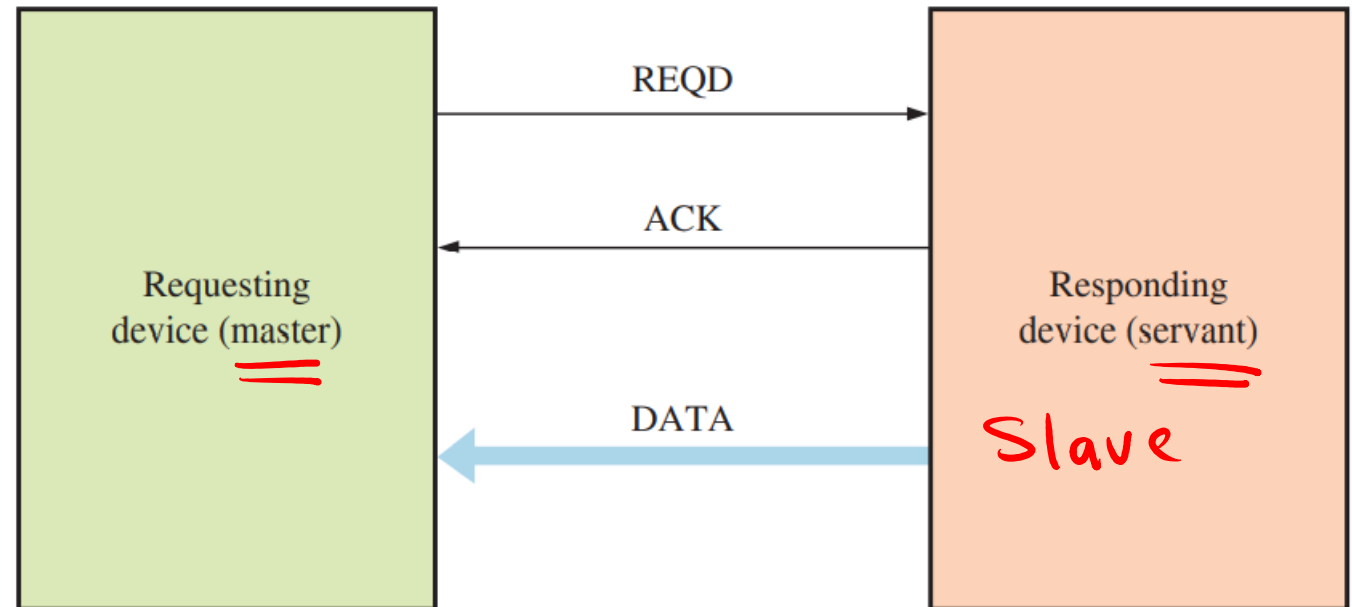
Handshaking

Asynchronous
Bus

- The handshake is a routine by which two devices initiate and complete a bus transfer.



- ① Master sends request for data (REQD) to servant.
- ② Servant sends an acknowledgement (ACK) and places data on bus.
- ③ Master receives data and removes request.
- ④ Servant removes acknowledge and is ready for next request.



| Synchronous and asynchronous Bus

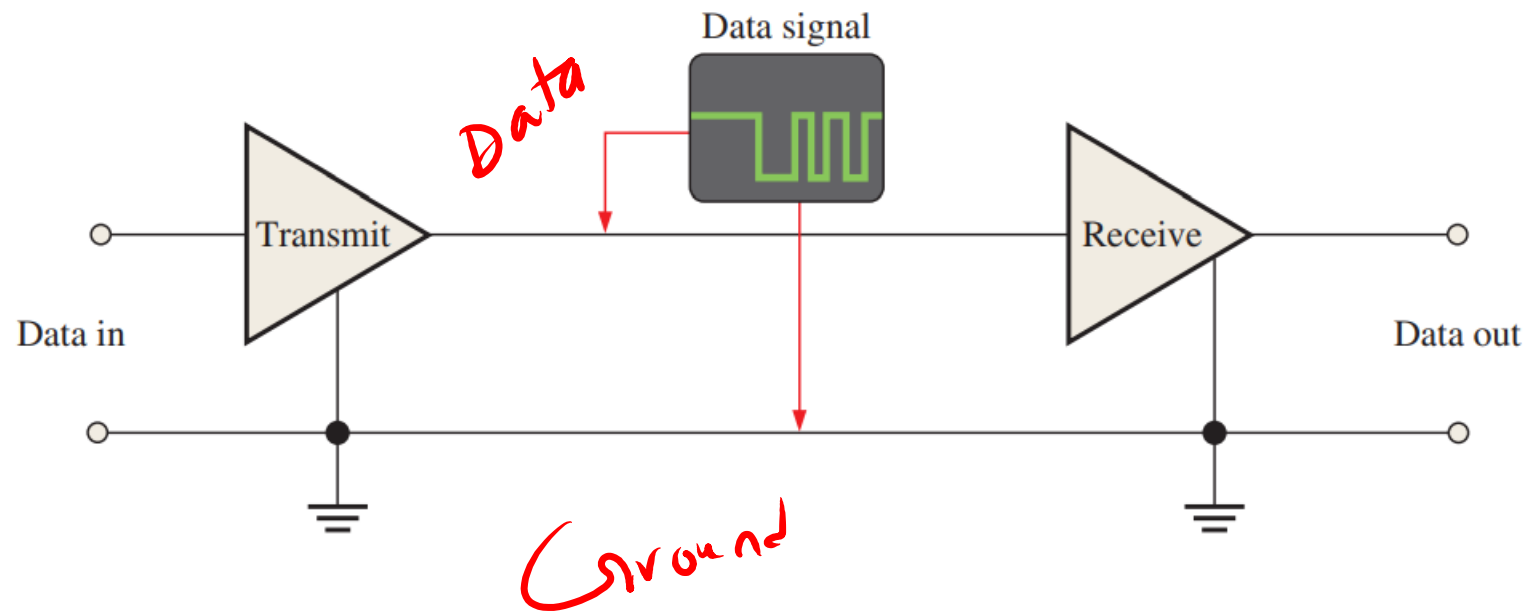
- A **synchronized bus** includes a **clock** in the control lines and has a fixed protocol that is relative to the clock.
- A synchronous bus is **fast** but has the disadvantage that every device connected to it must operate at the same clock frequency.
- Also, the **physical length** of the bus may be limited because of having to carry a **high-frequency clock signal.**
- An **asynchronous bus** is **not clocked**, so it can serve various devices with different clock rates.
- The asynchronous bus uses a **handshake** protocol to establish communication

| Single-Ended vs. Differential Buses

- Data communications between devices can be classified as either **single-ended** or **differential** in terms of the physical bus configuration.
- In general, **single-ended operation** is limited in both data rate and distance (cable length).
- Single-ended operation uses one wire for data and one wire for ground, where the signal voltage on the wire is with respect to ground

| Single-Ended vs. Differential Buses

- single-ended transmission is **simpler and lower in cost** compared to a differential transmission

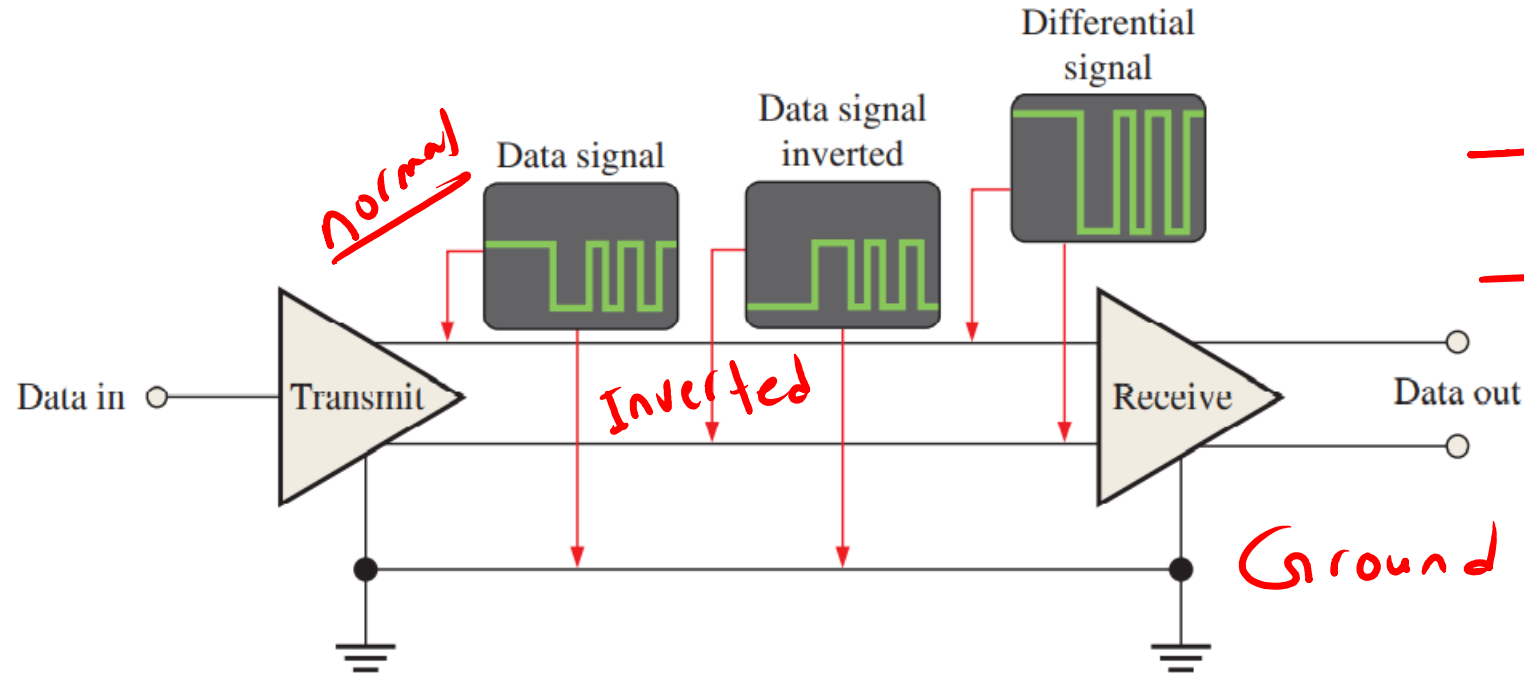


| Single-Ended vs. Differential Buses

- Differential operation provides much higher data rates and longer transmission distances
- Differential operation uses two wires for data and one wire for ground. The data signal is sent on one wire in the twisted pair and its complement (inversion) is sent on the other wire. The difference between the two data wires is the differential signal
- Differential operation is much less sensitive to noise because of common-mode rejection

| Single-Ended vs. Differential Buses

- Due to the **twisted pair**, **crosstalk** is reduced at higher frequencies, thus allowing longer cables



→ Cross talk ⇒ Reduce
→ longer cables