Chapter 3
A Top-Level View of Computer Function And Interconnection – Part 03

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Bus Interconnections

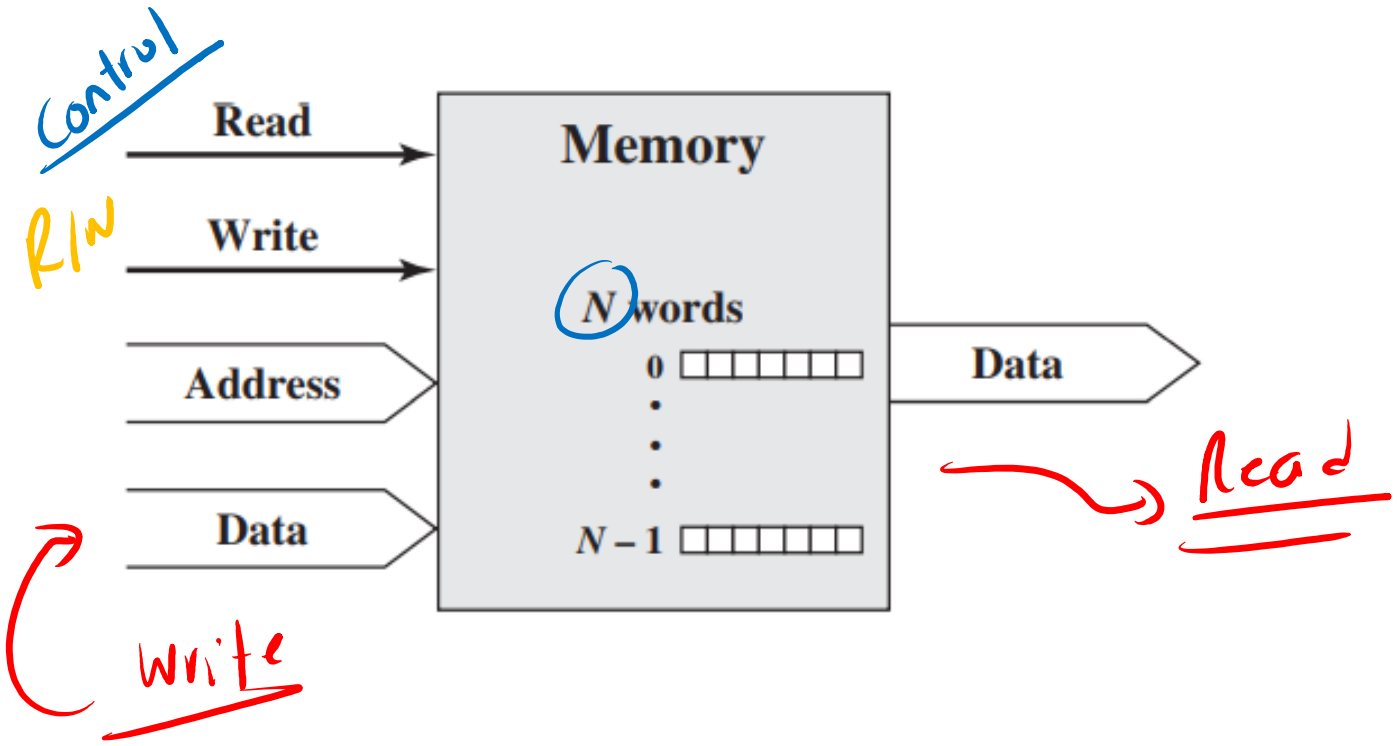
Agenda

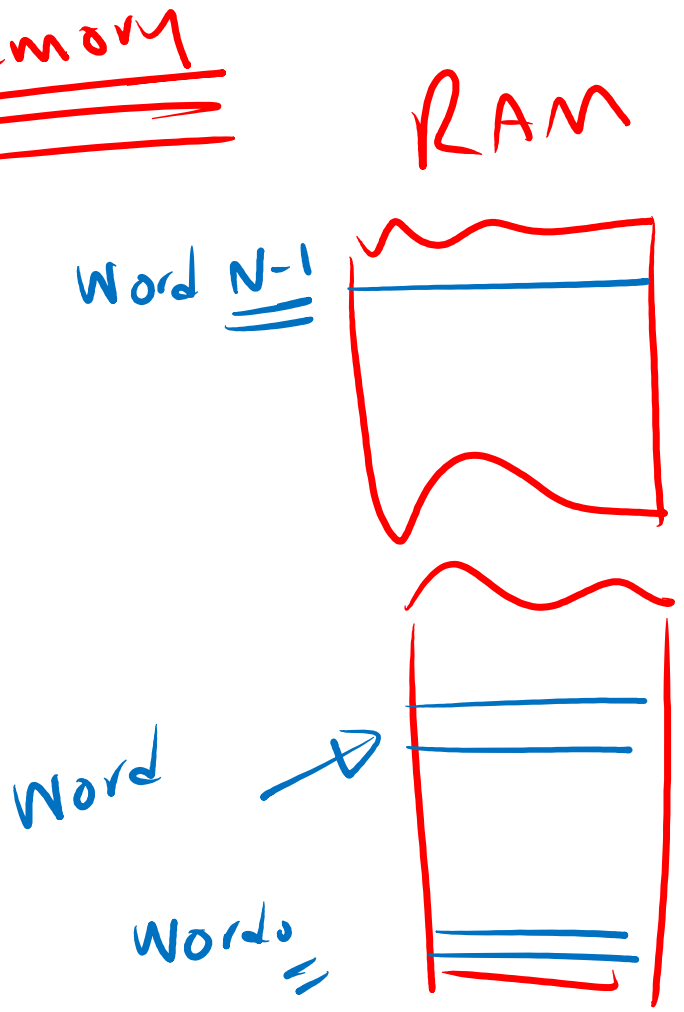
- Intro
- Computer Modules
  - Memory
  - I/O
  - CPU
- Buses
- System Bus
- Multiple-bus Hierarchies
- Bus Types

Intro…

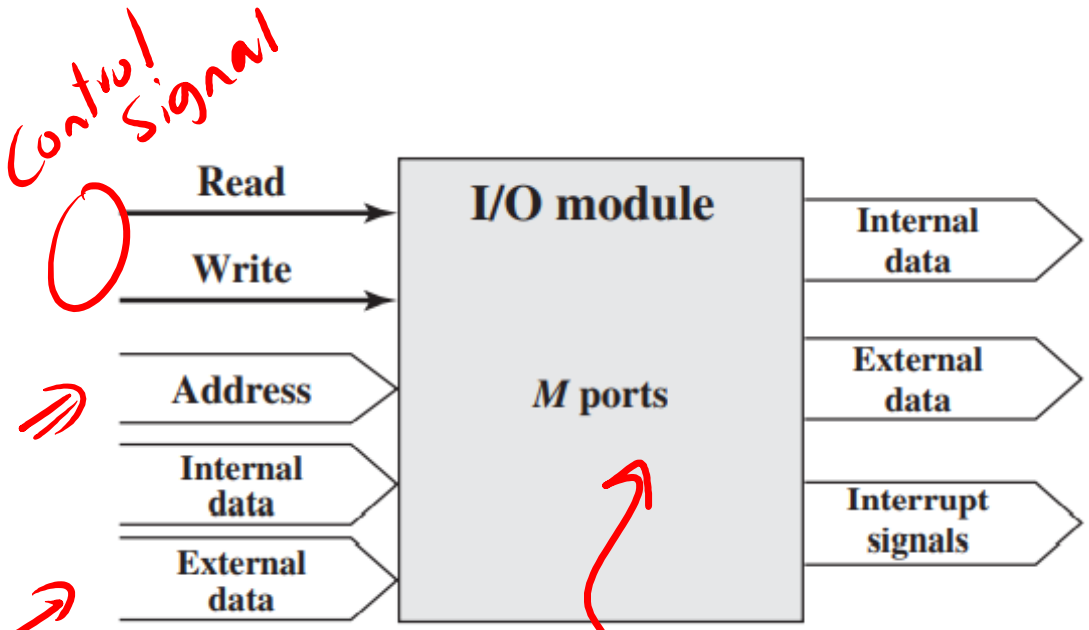
- A computer consists of a set of components or modules of three basic types:
  - CPU,
  - Memory,
  - I/O
- There must be paths for connecting the modules
- The collection of paths connecting the various modules is called the interconnection structure

Computer Modules

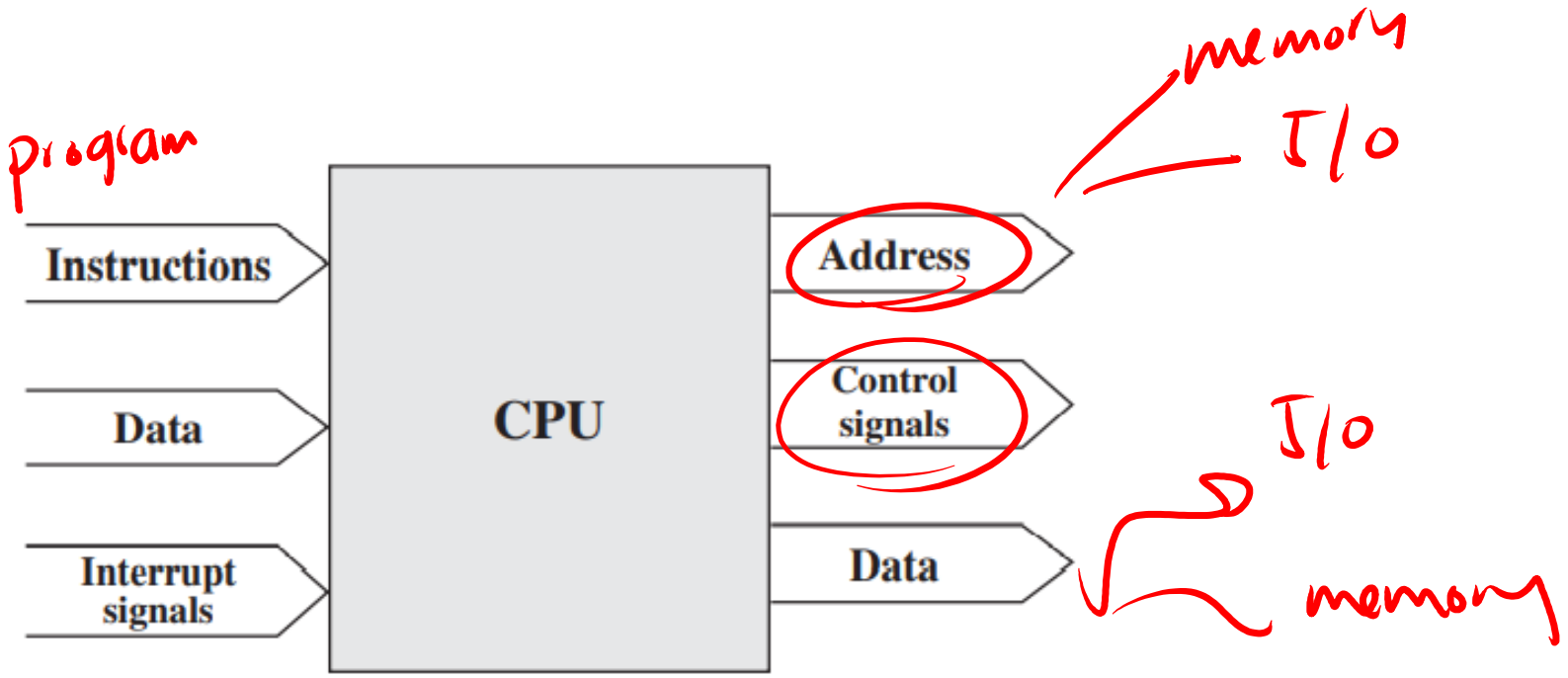




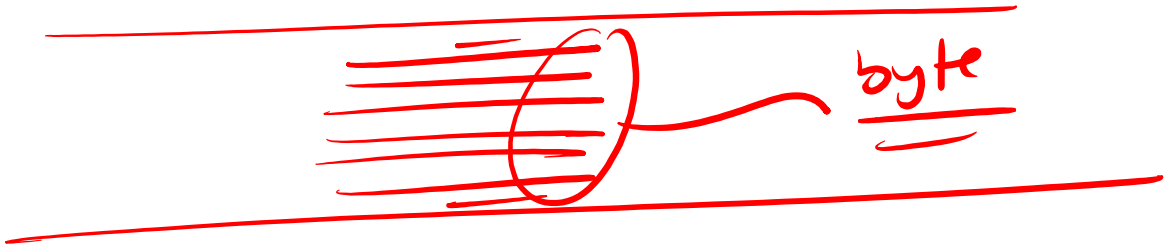
Computer Modules



Computer Modules

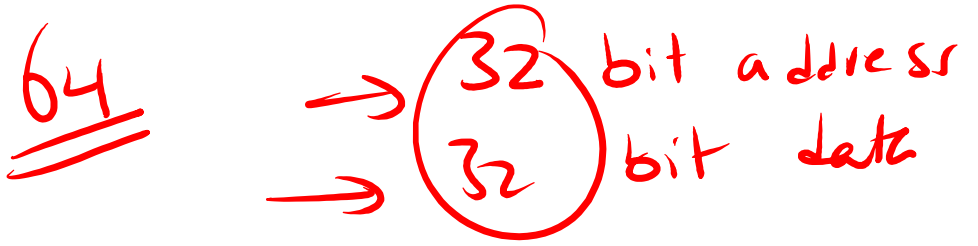


Buses



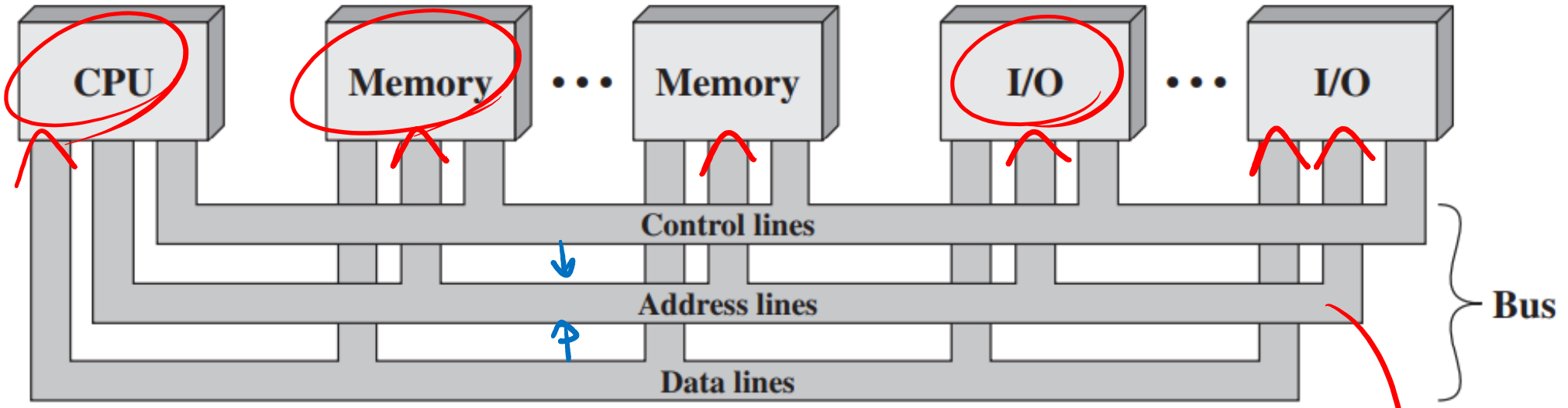
- A bus is a communication pathway connecting two or more devices.
  - Each line is capable of transmitting signals representing binary 1 and binary 0
  - 8-bit unit of data can be transmitted over eight bus lines.
- A key characteristic of a bus is that it is a shared transmission medium
  - Signal transmitted by any one device is available for reception by all other devices attached to the bus.
- Only one device at a time can successfully transmit

Buses



- A bus that connects major computer components (processor, memory, I/O) is called a system bus.
- The most common computer interconnection structures are based on the use of one or more system buses
- A system bus consists, typically, of from about 50 to hundreds of separate lines. Each line is assigned a particular meaning or function
- On any bus the lines can be classified into Data, Address, and Control lines. In addition, there may be power distribution lines

Bus Interconnection Scheme



0000 0000

0 memory ← 128 byte

1 I/O 128 byte

Address bus ↑ ⇝ memory size ↑

Data bus ↑ ⇝ performace ↑

unidirectional bus

Address Bus

- Identify the source or destination of data
  - CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity
- 8080 has 16-bit address bus giving 64k address space
- The address lines are generally also used to address I/O ports
  - 01111111 might reference locations in a memory module (module 0)
  - 10000000 and above refer to devices attached to an I/O module (module 1)

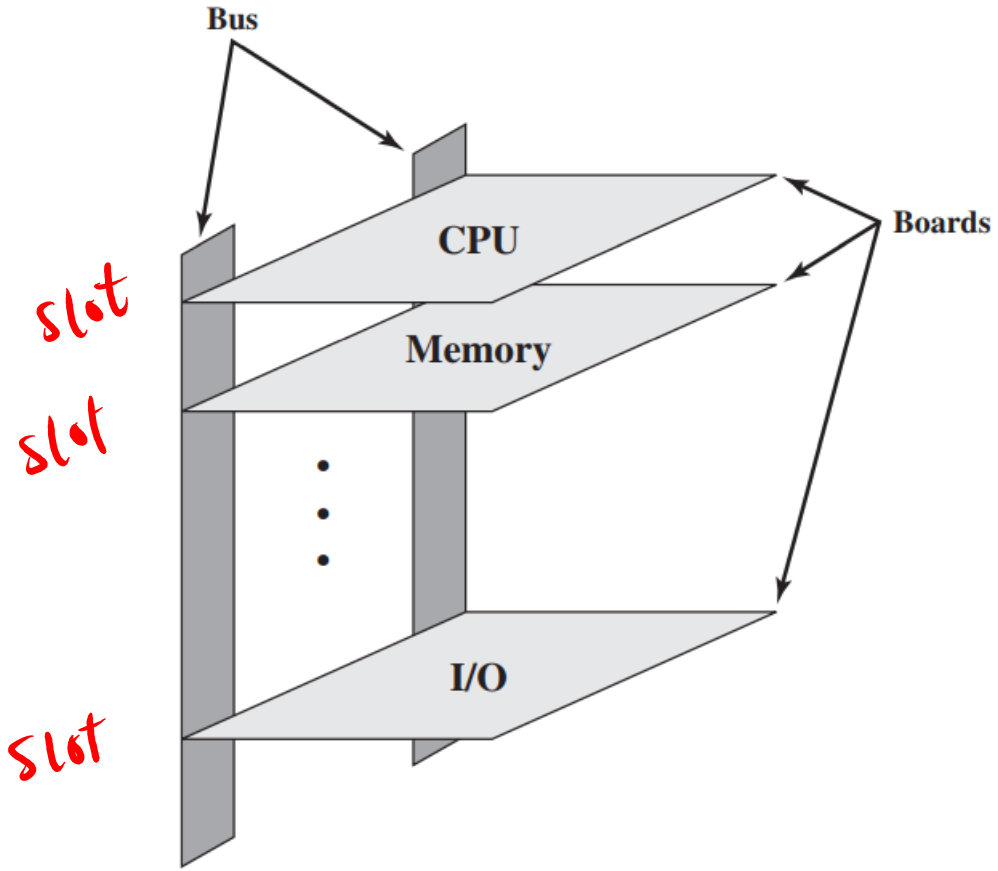
Control Bus

- The control lines are used to control the access to and the use of the data and address lines.
- Because the data and address lines are shared by all components, there must be a means of controlling their use
- Control signals transmit both command and timing information among system modules
  - Memory read/write signal
  - Interrupt request
  - Clock signals

Bus Request

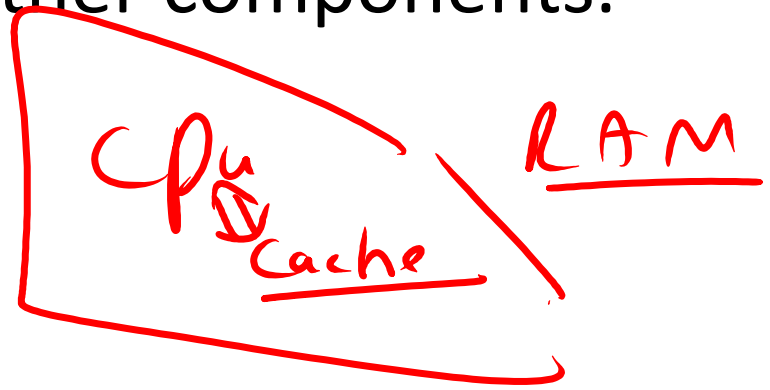
Bus grant

System Bus



Multiple-Bus Hierarchies

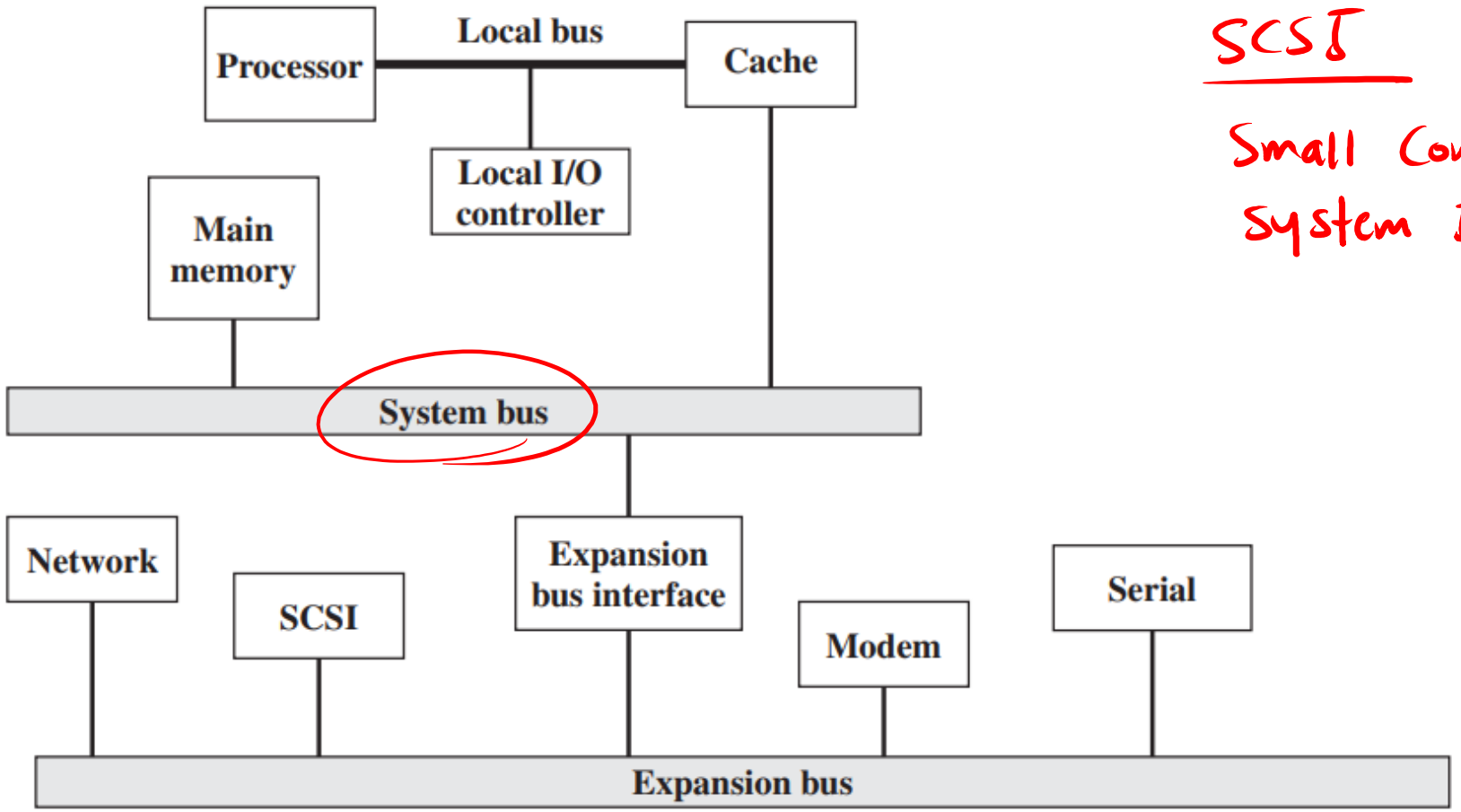
- Modern systems tend to have all of the major components on the same board with more elements on the same chip as the processor.
- Thus, an on-chip bus may connect the processor and cache memory, whereas an on-board bus may connect the processor to main memory and other components.



Single-Bus Problems

- Propagation delays
  - In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay
  - Long data paths mean that co-ordination of bus use can adversely affect performance
  - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Traditional bus architecture



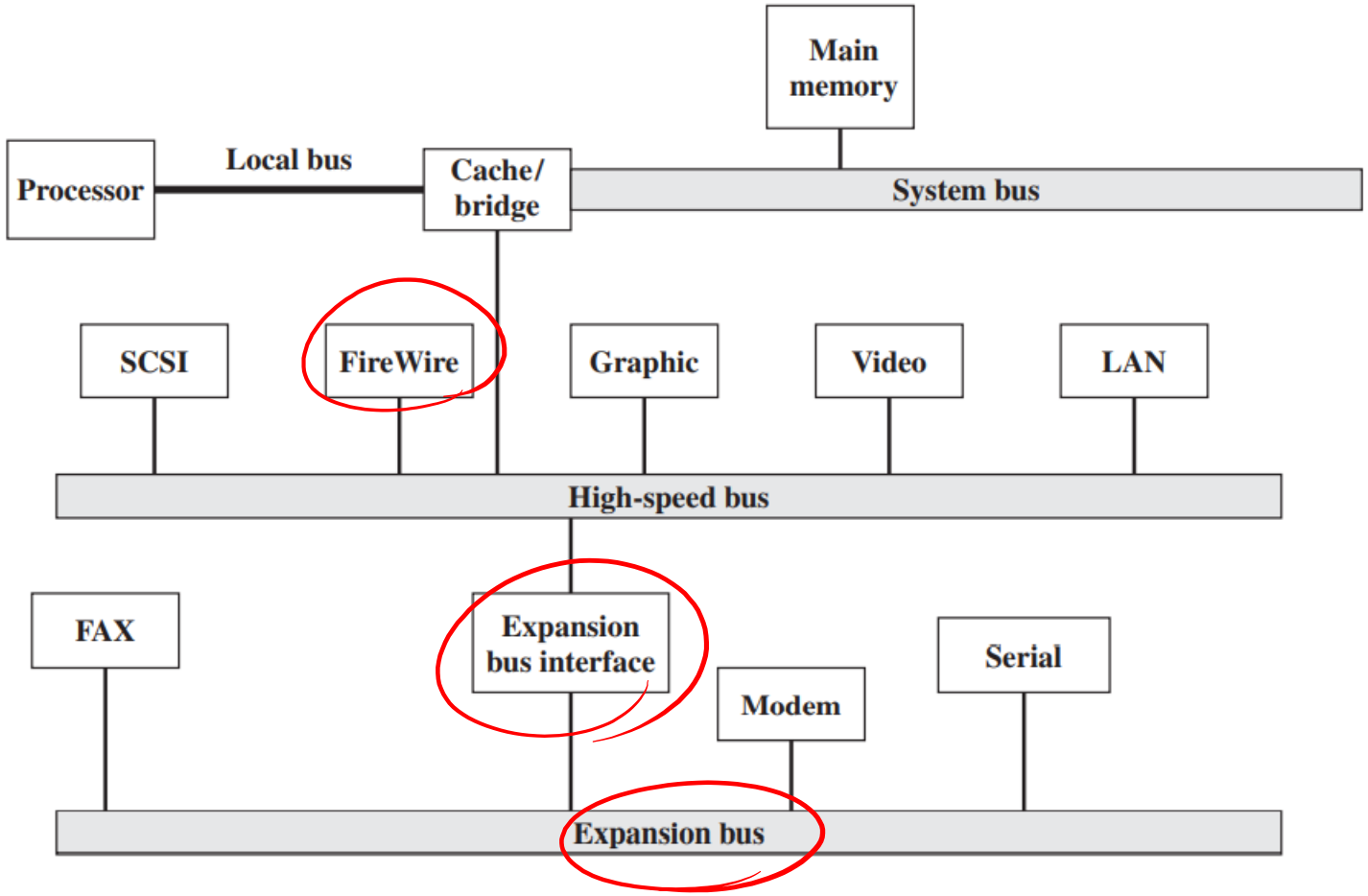
SCSI

Small Computer System Interface

bus

disk drive

High-performance architecture



Bus Types

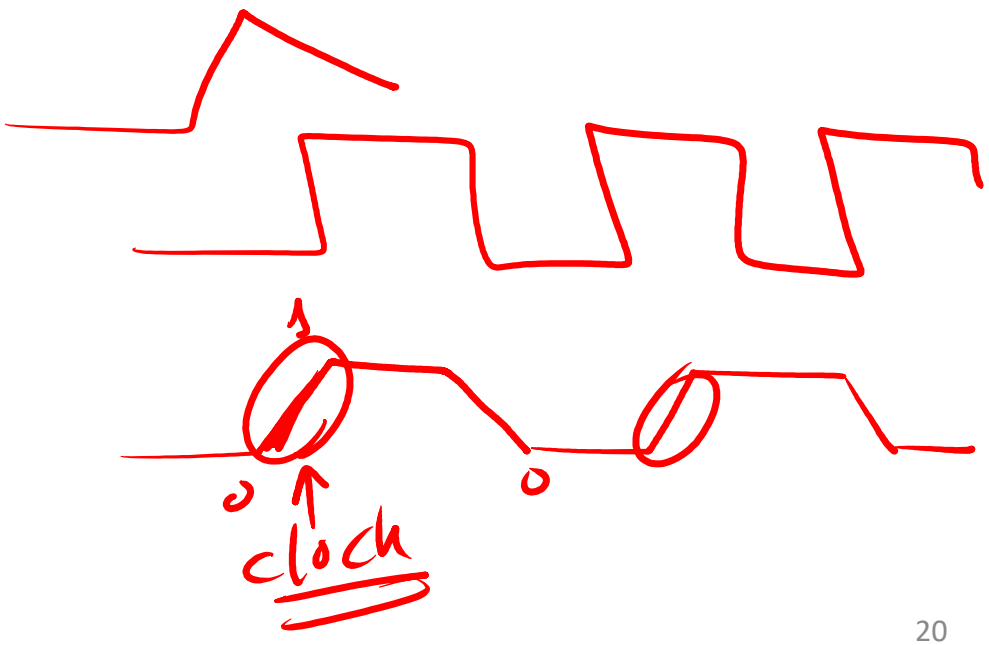
- A dedicated bus line is permanently assigned either to one function or to a physical subset of computer components
  - Separate data & address lines
  - Physical dedication: I/O to interconnect all I/O modules
- Multiplexed
  - Shared lines – Time Multiplexing
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
  - More complex control
  - Ultimate performance

Bus Arbitration

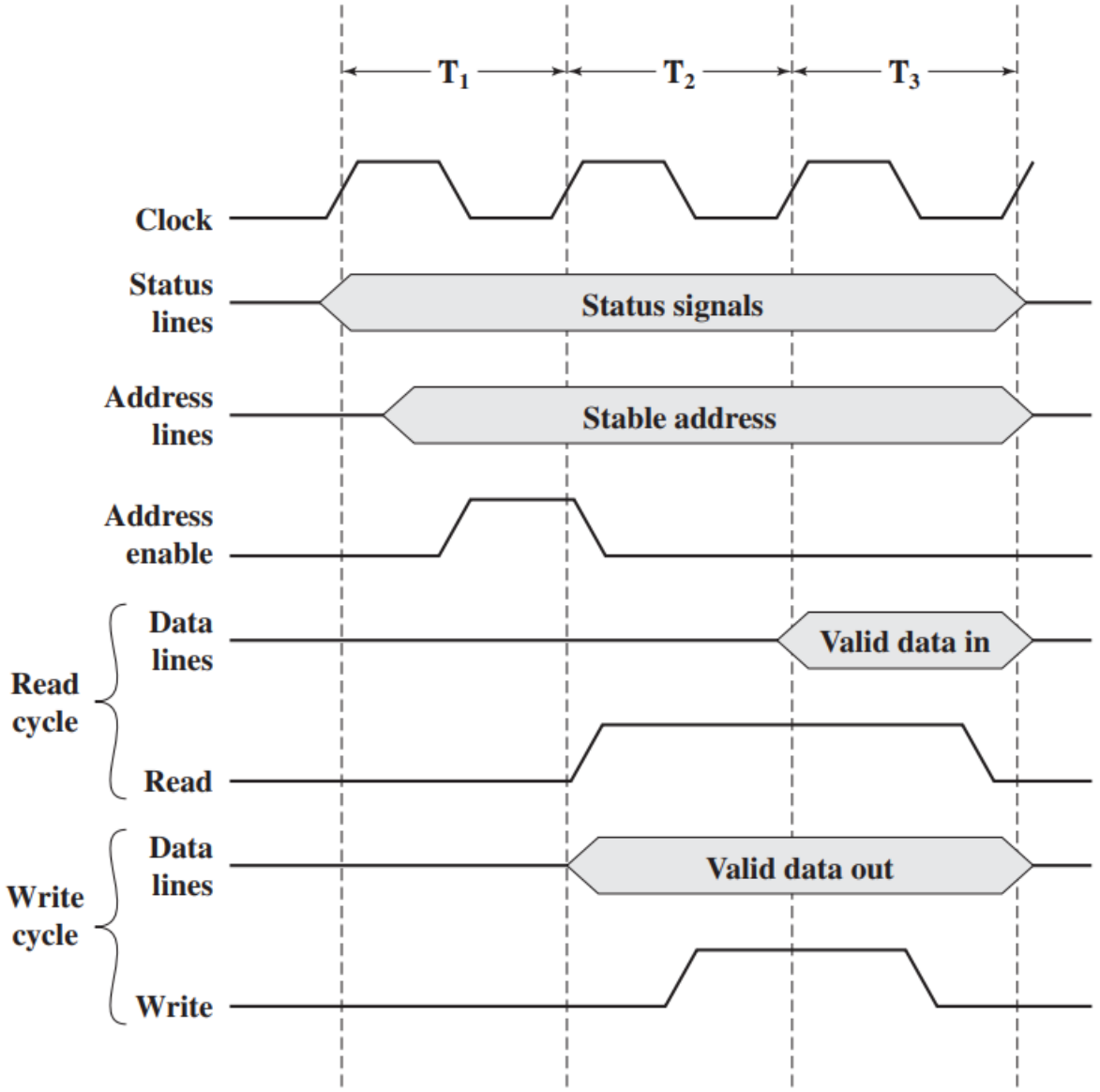
- More than one module may need control of the bus
- Because only one unit at a time can successfully transmit over the bus, some method of arbitration is needed
- In a centralized scheme, a single hardware device, referred to as a bus controller or arbiter, is responsible for allocating time on the bus. The device may be a separate module or part of the processor
- In a distributed scheme, there is no central controller. Rather, each module contains access control logic, and the modules act together to share the bus

Timing

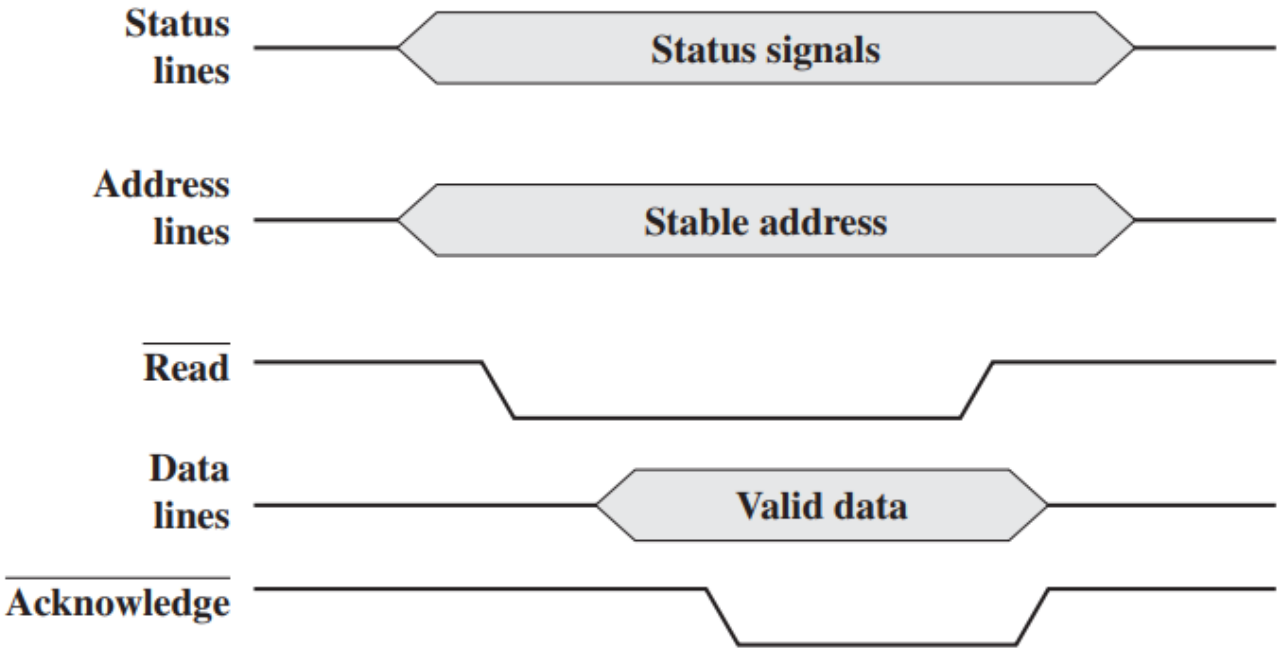
- Co-ordination of events on bus
- Synchronous
  - Occurrence of events on the bus is determined by a clock
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually, a single cycle for an event



Timing


T1
T2
T3
Clock
Status lines
Status signals
Address lines
Stable address
Address enable
Read cycle
Data lines
Valid data in
Read
Write cycle
Data lines
Valid data out
Write

Asynchronous - Read



Asynchronous - Write