COA

Chapter 04: | Associative Mapping

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AGENDA

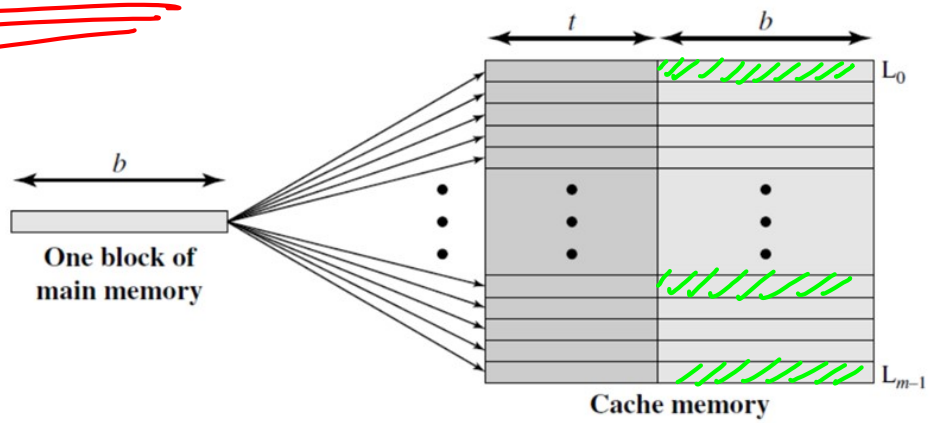
Elements of Cache Design

- Mapping Function
  - Direct
  - Associative
  - Set Associative

Cache Address
Cache size
Cache mapping
— Direct mapping

Associative Mapping

- Overcomes the disadvantage of direct mapping by **permitting** each main memory block to be **loaded into any line of the cache**



lines = m

Associative Mapping

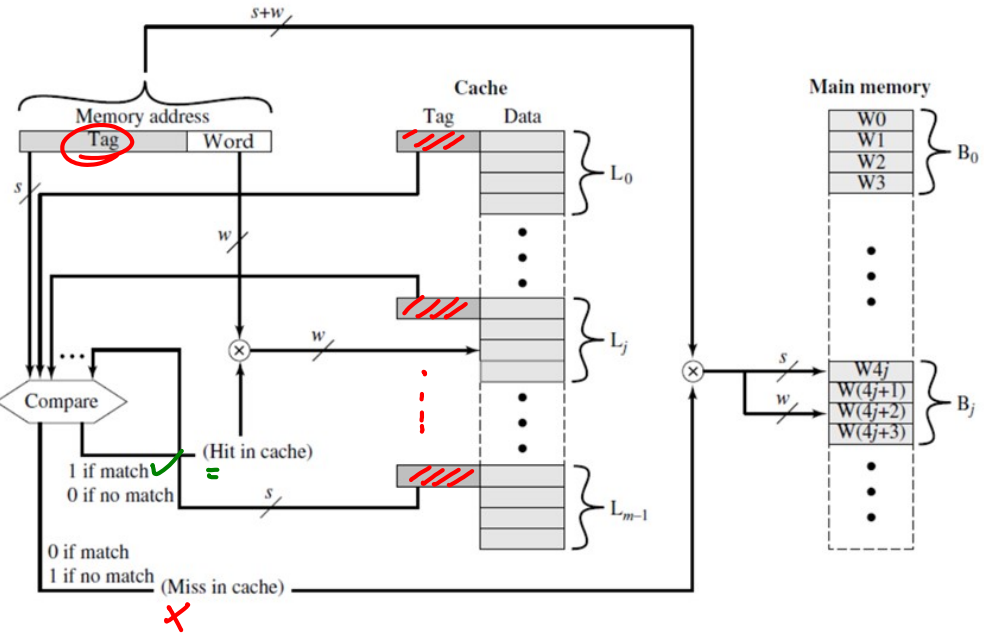
- The cache control logic interprets a **memory address** simply as a **Tag** and a **Word** field.
  - The **Tag field** uniquely identifies a **block of main memory**.
  - To determine **whether a block is in the cache**, the cache control logic must **simultaneously examine** every line's tag for a match

Access specific word

2-bit ⇒ 1-out of 4 words

4-bit ⇒ 1-out of 16 words

Associative Mapping



Very Complex

Block

Block size = 4 words

W

0 0 ⇒ Word 0

0 1 ⇒ Word 1

↓

1 1 ⇒ Word 3

Associative Mapping

To Summarize:

- Address length: $s + w$ bits
- Number of addressable units: 2^{s+w} words or bytes
- Block size = line size = 2^{w} words or bytes
- Number of blocks in main memory: $\frac{2^{s+w}}{2^{w}} = 2^{s}$
- Number of lines in cache = undetermined
- Size of tag: s bits
  - No field in the address corresponds to the line number

Associative Mapping

- Cache size : 64 Kbytes.
- Block size: 4 bytes.
- Cache is organized as $16\,K = 2^{14}$ lines of 4 bytes each.
- Memory Size: 16 Mbytes, with each byte directly addressable by a 24-bit address ($2^{14} = 16\,M$).
  - Main memory: 4M blocks of 4 bytes each

$2^{16}/2^2 \Rightarrow 2^{14}$ cach line

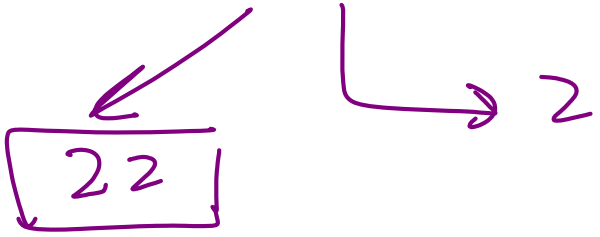
$\Rightarrow w = 2$

24

$\Rightarrow 2$

$\Rightarrow$ Address = 24 bit

S+W = 24



Example

word 0

Memory address	0001 0110 0011 0011 1001 1100 (binary)	⇒ memory Address
1 6 3 3 9 C (hex)	0 5 8 C E 7	
Tag (leftmost 22 bits)	00 0101 1000 1100 1110 0111 (binary)	⇒ Tag
0 5 8 C E 7 (hex)		

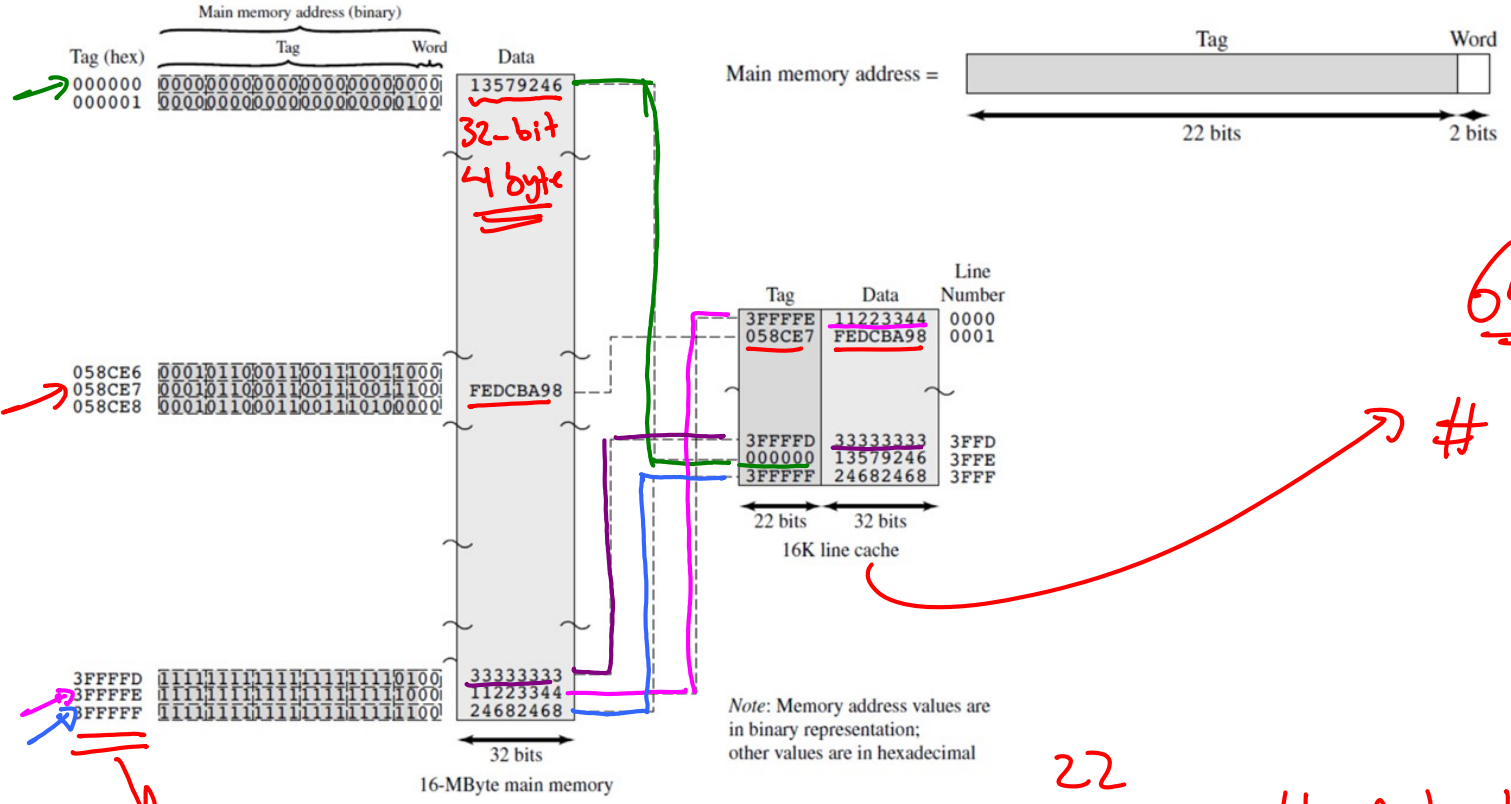
6-digit ⇒ 24 bit ⇒ 2^{24} ⇒ 16 mbyte

24-bit ⇒ S+W

S → 22

W → 2

22 = Tag



64 Kbyte = 2^{16}

line = $2^{16}/2^{2} = 2^{14}$

= 16 K line

11 1111 1111 1111 1111 1111 ⇒ 22-bit ⇒ 2^{22} ⇒ 4 Mbyte block

Associative Mapping Pros & Cons

- With associative mapping, there is **flexibility** as to which block to replace when a new block is read into the cache.
  - **Replacement algorithms** are designed to maximize the hit ratio.
- **Complex circuitry** required to **examine the tags** of all cache lines in parallel.