COA

Chapter 05: | DRAM - SRAM

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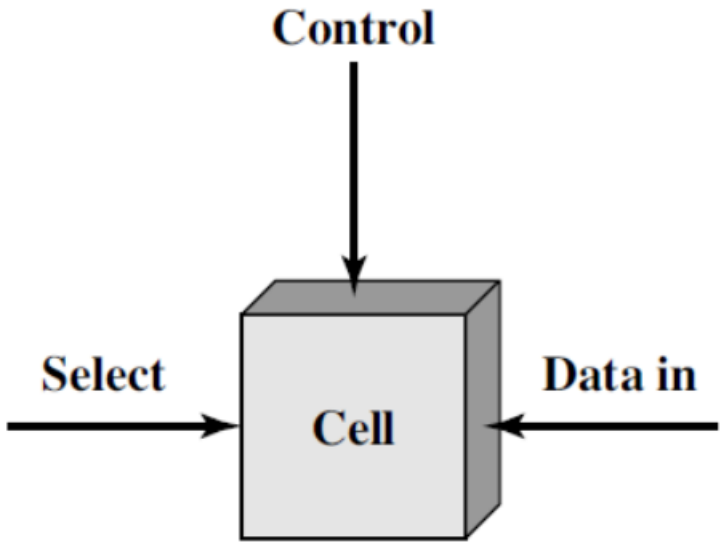
AGENDA

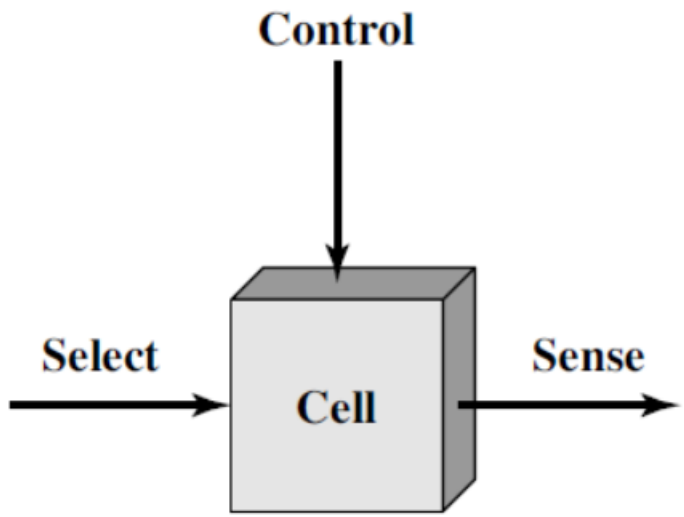
- Organization
- DRAM and SRAM

Organization

- The basic element of a semiconductor memory is the **memory cell**
  - Select
  - Control



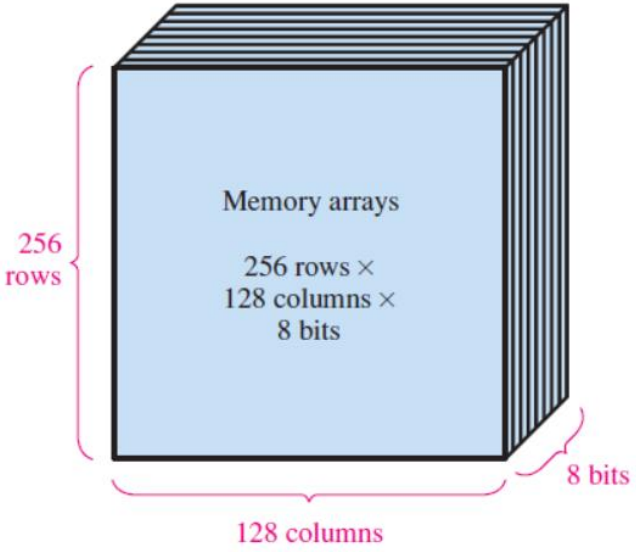
(a) Write



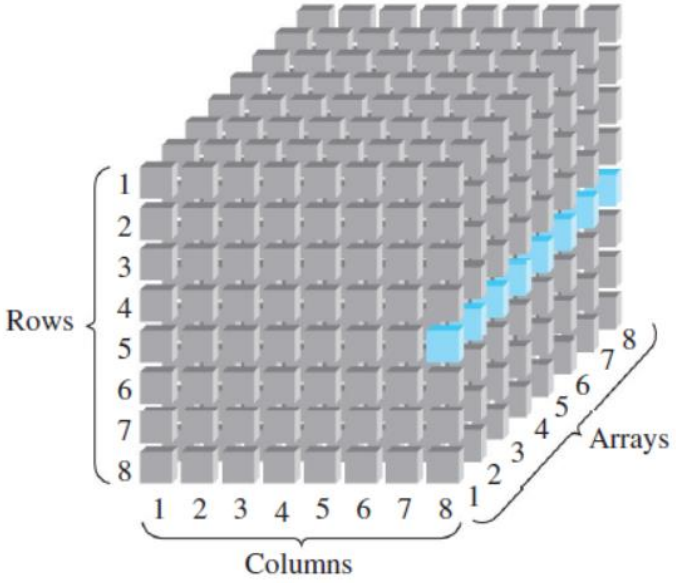
(b) Read

Organization

- **SRAM chips** can be organized in **single bits**, **nibbles** (4 bits), **bytes** (8 bits), or multiple bytes (words with 16, 24, 32 bits, etc.)



(a) Memory array configuration

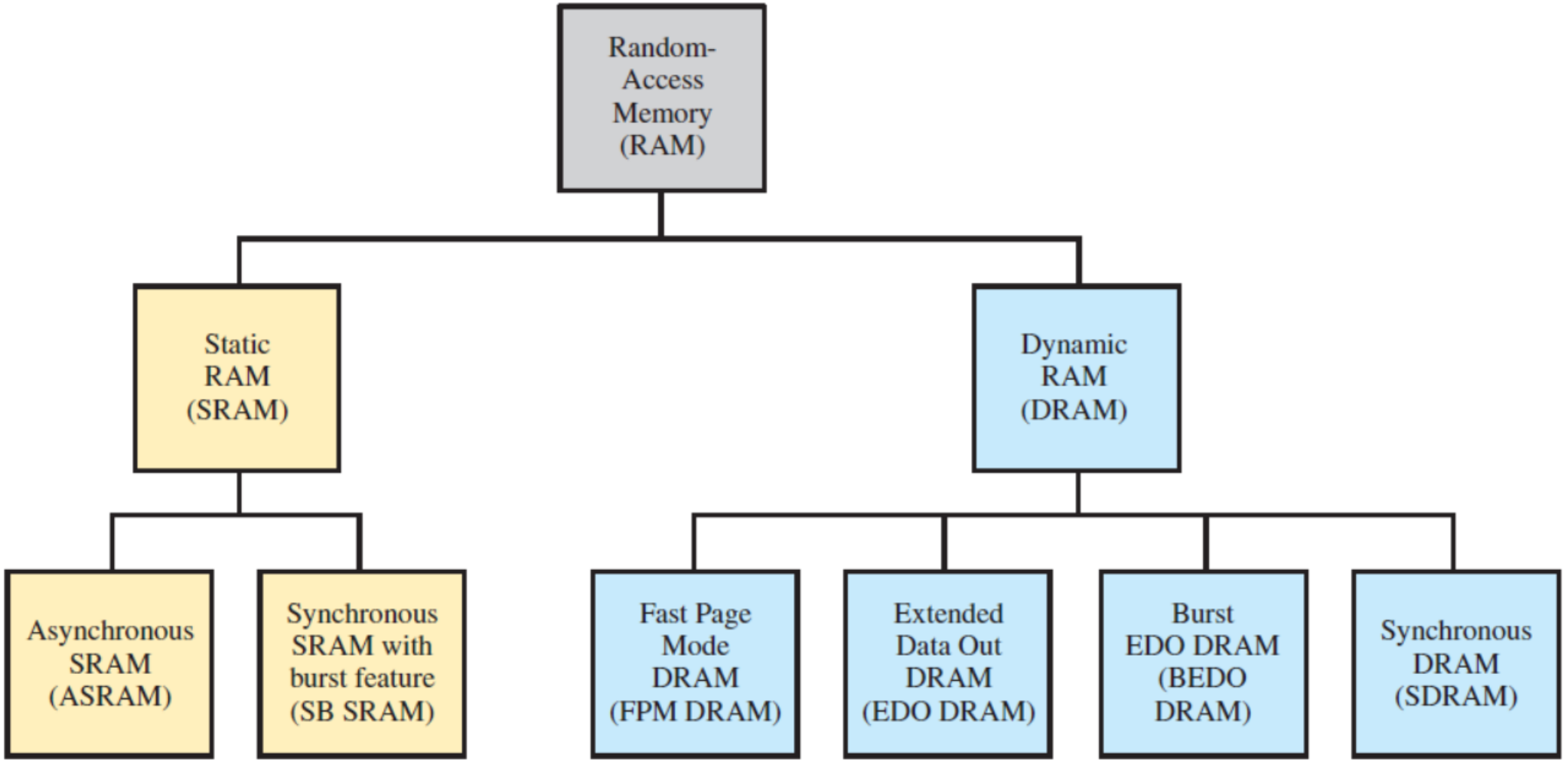


(b) The address of the blue byte is row 5, column 8.

Random Access

- All of the memory types that we will explore in this chapter are **random access**
- Individual words of memory are **directly accessed** through wired-in addressing logic
- The **most common** is referred to as random-access memory (**RAM**)

DRAM & SRAM

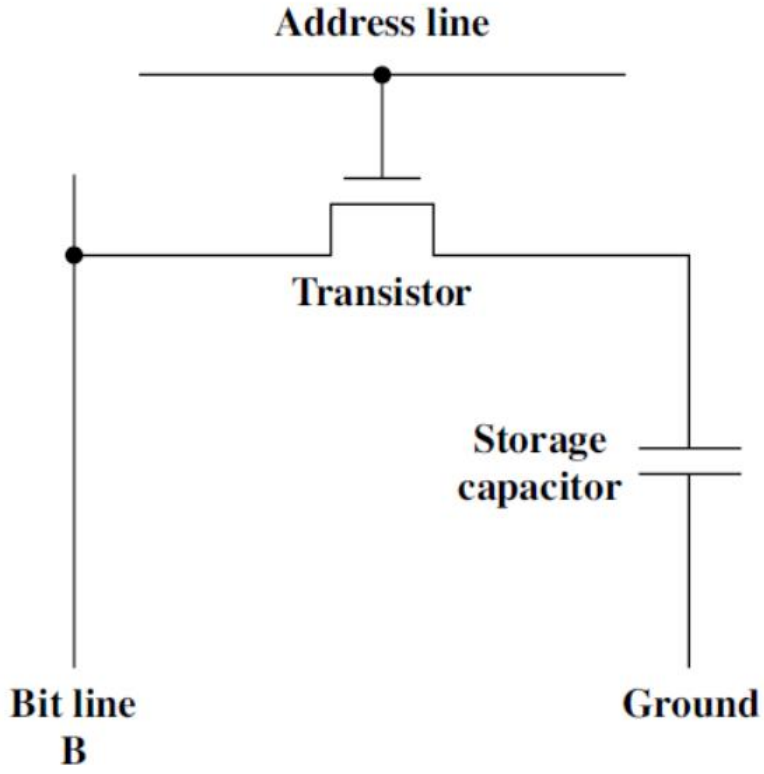

Random-Access Memory (RAM)
Static RAM (SRAM)
Dynamic RAM (DRAM)
Asynchronous SRAM (ASRAM)
Synchronous SRAM with burst feature (SB SRAM)
Fast Page Mode DRAM (FPM DRAM)
Extended Data Out DRAM (EDO DRAM)
Burst EDO DRAM (BEDO DRAM)
Synchronous DRAM (SDRAM)

RAM

- **RAM** is also referred to as **RAWM** (**Read And Write Memory**)
- **RAM** memory is **volatile** memory
  - **cutting off** the power to the IC results in the **loss of data**
- There are three types of RAM
  - Static RAM (**SRAM**)
  - NV-RAM (Nonvolatile RAM)
  - Dynamic RAM (**DRAM**)

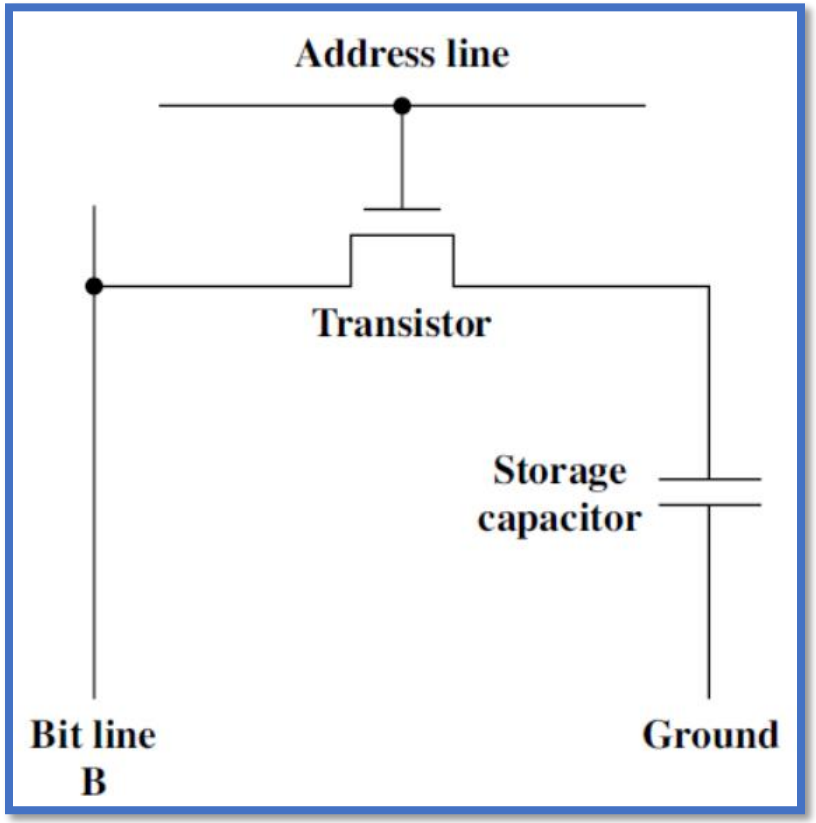
Dynamic RAM (DRAM)

- Store data as **charge on capacitors**.
  - Using a capacitor – cuts down the number of transistors
- The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0
- Capacitor **charge dissipates** over time causing a 1 to flip to a zero
  - Refreshed



Dynamic RAM (DRAM)

- The **sense amplifier** compares the capacitor voltage to a reference value
- The **readout** from the cell discharges the capacitor
- DRAM is an **analog** device

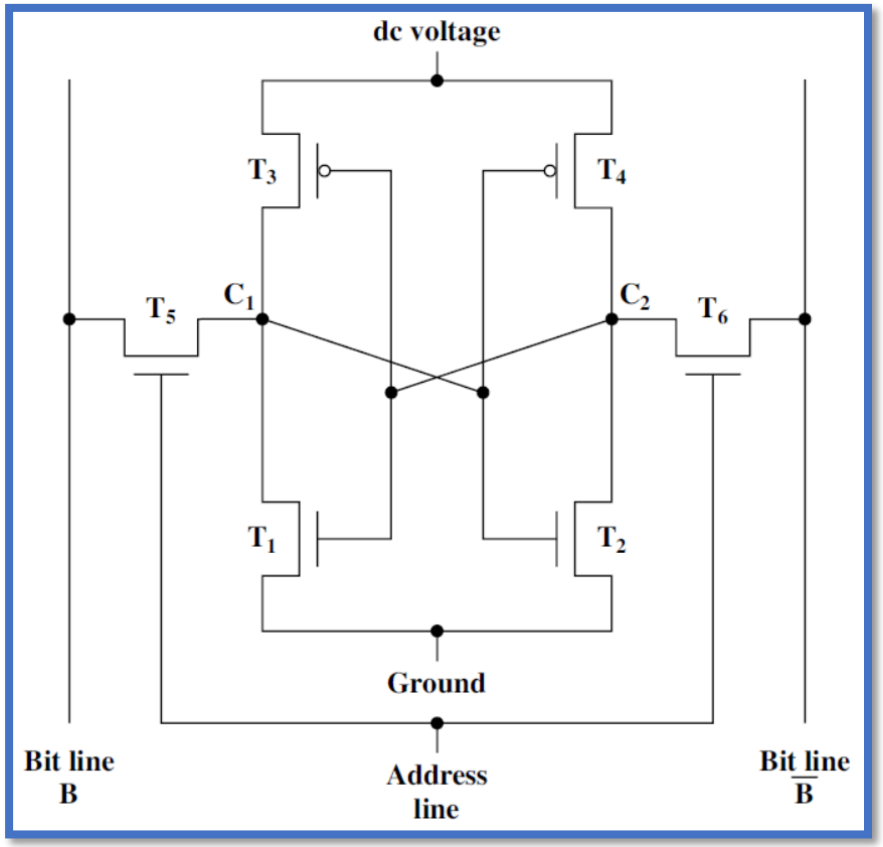


Dynamic RAM (DRAM)

- High density
  - store much more data than SRAMs for a given physical size and cost
- Cheaper cost per bit
- Lower power consumption
- It must be refreshed
- While DRAM is being refreshed, the data can not be accessed

Static RAM (SRAM)

- Basically an array of flip-flop storage cells
  - Each cell requires at least 6 transistors (may be 4)
- **Faster** than a dynamic cell



SRAM Vs. DRAM

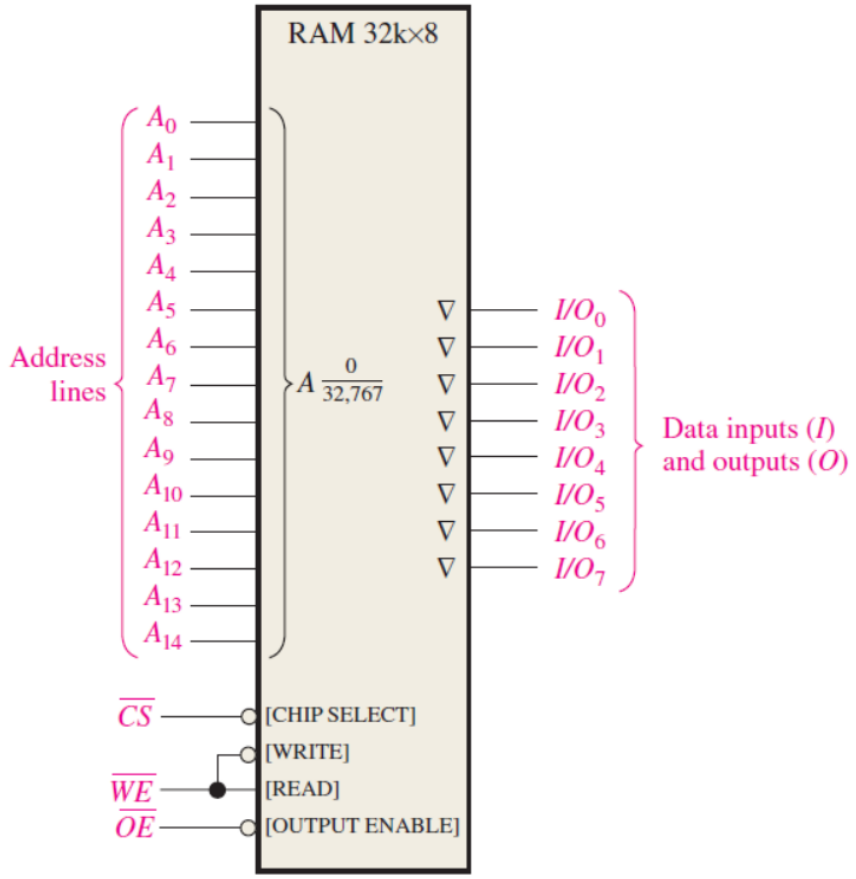
- Data can be **read much faster from SRAMs** than from DRAMs.
- **DRAMs can store much more data than SRAMs for a given physical size and cost**
- **DRAM** is more **dense** (smaller cells = more cells per unit area) and **less expensive** than a corresponding SRAM
- **DRAM** requires the supporting **refresh circuitry**

SRAM Vs. DRAM

- DRAMs tend to be favored for large memory requirements
  - fixed cost of the refresh circuitry is more than compensated for by the smaller variable cost of DRAM cells
- **SRAM** is used for **cache memory** (both on and off chip), and **DRAM** is used for **main memory**

Basic Asynchronous SRAM Organization

- Operation is not synchronized with a system clock



Logic diagram for an asynchronous 32k × 8 SRAM.