COA

Chapter 05: | Advanced DRAM Organization

Prof. Dr. Mostafa Elhosseini

https://youtube.com/drmelhosseini

AGENDA

- Synchronous DRAM (SDRAM)
- Double Data Rate SDRAM (DDR-SDRAM)
- Rambus DRAM (RDRAM)
- Cache DRAM (CDRAM)

Intro…

- One of the most **critical system bottlenecks** when using high-performance processors is the interface to main internal memory
- The **basic building block** of main memory remains the **DRAM** chip
  - Insert one or more levels of high-speed **SRAM cache**
  - **SRAM** is much **costlier** than DRAM

DRAM Improvements

- Synchronous DRAM (SDRAM)
- Double Data Rate SDRAM (DDR-SDRAM)
- Rambus DRAM (RDRAM)
- Cache DRAM (CDRAM)

DRAM

- **DRAM** is **asynchronous**
  - **With asynchronous memories**, the **microprocessor** must **wait** for the DRAM to complete its internal operations
- **Faster DRAMs** are needed to keep up with the ever-increasing speed of microprocessors

Synchronous DRAM (SDRAM)

- **SDRAM** Access is **synchronized** with an **external clock**
- with synchronous operation, the **DRAM latches** addresses, data, and control information from the processor under control of the system clock.
  - CPU does not have to wait; it can do something else

Synchronous DRAM (SDRAM)

- The **SDRAM** employs a **burst mode** to eliminate the address setup time and row and column line precharge time after the first access
  - Burst mode allows SDRAM to set up stream of data and fire it out in block
- SDRAM has a **multiple-bank** internal architecture that improves opportunities for on-chip parallelism

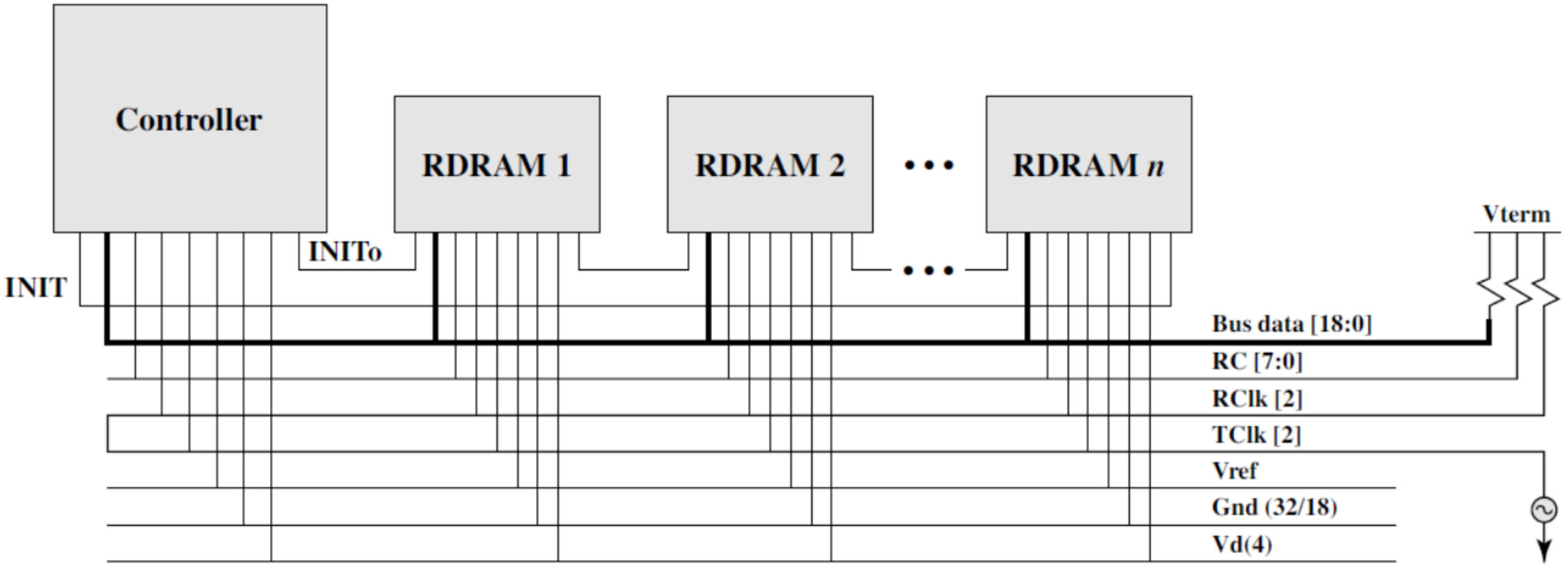
Synchronous DRAM (SDRAM)

- The **mode register** and **associated control logic** is another key feature differentiating SDRAMs from conventional DRAMs
  - It provides a mechanism to **customize the SDRAM** to suit specific system needs.
  - The **mode register** specifies the **burst length**, which is the number of separate units of data synchronously fed onto the bus
  - The register also allows the programmer to **adjust the latency** between receipt of a read request and the beginning of data transfer
  - The **SDRAM performs best** when it is **transferring large blocks** of data serially, such as for **applications** like **word** processing, **spreadsheets**, and **multimedia**

Rambus DRAM (RDRAM)

- Adopted by Intel for Pentium & Itanium
- Main competitor to SDRAM
- Vertical package – all pins on one side
- Data exchange over 28 wires < 12 cm long
- Bus addresses up to 320 RDRAM chips at 1.6Gbps
- Asynchronous block protocol
  - 480ns access time
  - Then 1.6 Gbps

Rambus DRAM (RDRAM)



Double Date Rate (DDR) SDRAM

- **DDR** stands for **double data rate**.
- DDR-SDRAM sends data twice per clock cycle (**leading** & **trailing** edge)
  - rising edge and the falling edge
- whereas a SDRAM is clocked on only one edge. Because of the double clocking, a DDR SDRAM is **theoretically twice as fast as an SDRAM**.
  - widely used in desktop computers and servers

Double Date Rate (DDR) SDRAM

- Sometimes the **SDRAM** is referred to as an **SDR SDRAM** (**s**ingle **d**ata **r**ate **SDRAM**) for contrast with the DDR SDRAM
- There have been two generations of improvement to the DDR technology
  - DDR2
  - DDR3

Cache DRAM (CDRAM)

- **Cache DR**AM (CDRAM), developed by Mitsubishi **integrates** a **small SRAM** cache (16 Kb) onto a generic **DRAM chip**
- The SRAM on the CDRAM can be used in two ways
- true cache
- buffer to support the serial access of a block of data

Other types of DRAMs

- Fast Page Mode (FPM) DRAM
- Extended Data Out (EDO) DRAM
- Burst Extended Data Out (BEDO) DRAM