College of Computer Science & Engineering at Yanbu.

جامعة طيبة
TAIBAH UNIVERSITY

كلية علوم وهندسة الحاسبات بينبع

Department of Computer Science.

قسم علوم الحاسبات

Midterm. Exam 02

Academic Year 1447 - Second Semester

Exam Information معلومات الامتحان			
Course name	**تنظيم وبناء الحاسب**		**اسم المقرر**
Course Code	**COE 224**		**رمز المقرر**
Exam Date	26 / 4 / 2026	**الأحد**	**تاريخ الامتحان**
Exam Time	12:00 – 13:00		**وقت الامتحان**
Exam Duration	1 Hour		**مدة الامتحان**
Classroom No.	**GF 16**		**رقم قاعة الاختبار**
Instructor Name	**Prof. Dr. Mostafa Elhosseini**		**اسم استاذ المقرر**

Student Information معلومات الطالب		
Student's Name		**اسم الطالب**
ID number		**الرقم الجامعي**
Section No.		**رقم الشعبة**
Serial Number		**الرقم التسلسلي**

General Instructions:

تعليمات عامة:

- Your Exam consists of 3 PAGES (except this paper)
- Phones and smart devices are forbidden inside the hall.

- عدد صفحات الامتحان 3 صفحة. (بإستثناء هذه الورقة)
- يمنع استخدام الهواتف والأجهزة الذكية داخل القاعة.

هذا الجزء خاص بأستاذ المادة

This section is ONLY for instructors.

#	Course Learning Outcomes (CLOs)	Related Question (s)	Points	Final Score
4	Analyze, develop, and test MIPS assembly language programs	Q1	10	
5	Design the datapath of a single-cycle processor	Q2 – Part A	5	
6	Design the datapath of a pipelined processor and handle hazards	Q2 – Part B	5	

Question 1: Points: 10		CLO #4

For **MIPS Architecture**, answer the following MCQs.

1. What is the value of $t2?

```
li $t0, 10
li $t1, 4
sub $t2, $t0, $t1
```

   A. 6
   B. 14
   C. -6
   D. 40

2. What is the output?

```
li $a0, 7
li $v0, 1
syscall
```

   A. 0
   B. 1
   C. 7
   D. Error

3. What does **beq** do?
   A. Jump always
   B. Branch if equal
   C. Branch if not equal
   D. Load value

4. What does **j** label do?
   A. Conditional jump
   B. Function call
   C. Unconditional jump
   D. Load address

5. What does **.data** section store?
   A. Instructions
   B. Registers
   C. Variables
   D. Labels only

6. Which instruction **loads a word from memory**?
   A. sw
   B. lw
   C. la
   D. li

7. In MIPS, how can you implement **NOT $t1**?
   A. and $t0, $t1, $t1
   B. nor $t0, $t1, $zero
   C. or $t0, $t1, $zero
   D. xor $t0, $t1, $t1

8. What is the result of:

```
li $t0, 0b1101
li $t1, 0b0101
and $t2, $t0, $t1
```

   A. 1111
   B. 1001
   C. 0101
   D. 0001

9. What is the purpose of using **AND** in:
   and $t0, $t1, 0xFF
   A. Flip bits
   B. Clear upper bits
   C. Add numbers
   D. Shift left

10. Which instruction **sets the lowest bit of $t0 to 1**?
    A. and $t0, $t0, 1
    B. or $t0, $t0, 1
    C. xor $t0, $t0, 1
    D. nor $t0, $t0, 1

Question 2: Points: 10		CLO #5,6

Part A: Points 5 CLO #5

In **MIPS architecture**, **R-type instructions** are encoded using a 32-bit format consisting of the following fields: opcode (6 bits, always 0 for R-type), rs (5 bits, first source register), rt (5 bits, second

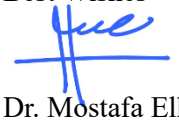
source register), rd (5 bits, destination register), shamt (5 bits, shift amount, assume 0 for add), and funct (6 bits, determines the operation). The register mapping is given as follows: $s0 = 16 (10000), $t2 = 10 (01010), and $t4 = 12 (01100). The function code for the add instruction is 32 (100000).

Given the MIPS instruction **add $s0, $t2, $t4**, construct the complete **32-bit machine code in binary**, and finally convert the result into **hexadecimal format**.

Part B: Points 5 CLO #6

11. What is the main goal of **pipelining**?
    A. Reduce instruction size
    B. Increase clock frequency only
    C. Improve throughput (more instructions per unit time)
    D. Reduce number of registers
12. A **structural hazard** occurs when:
    A. Two instructions need the same hardware resource at the same time
    B. One instruction depends on another
    C. A branch changes program flow
    D. Instruction format is incorrect
13. Which unit performs arithmetic operations in the datapath?
    A. Register File
    B. ALU
    C. Memory
    D. Control Unit
14. In pipelining, multiple instructions:
    A. Execute sequentially
    B. Execute partially in parallel
    C. Execute randomly
    D. Execute only one at a time
15. The hazard detection unit is responsible for:
    A. Performing ALU operations
    B. Detecting hazards and inserting stalls
    C. Accessing memory
    D. Writing result

Best Wishes



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