College of Computer Science & Engineering at Yanbu.

جامعة طيبة
TAIBAH UNIVERSITY

كلية علوم وهندسة الحاسبات بينبع

Department of Computer Science.

قسم علوم الحاسبات

Midterm. Exam 01

Academic Year 1447 - Second Semester

Exam Information معلومات الامتحان			
Course name	**تنظيم وبناء الحاسب**		**اسم المقرر**
Course Code	**COE 224**		**رمز المقرر**
Exam Date	1 / 3 / 2026	**الأحد**	**تاريخ الامتحان**
Exam Time	11:00 – 12:00		**وقت الامتحان**
Exam Duration	1 Hour		**مدة الامتحان**
Classroom No.	**GF 1**		**رقم قاعة الاختبار**
Instructor Name	**Prof. Dr. Mostafa Elhosseini**		**اسم استاذ المقرر**

Student Information معلومات الطالب		
Student's Name		**اسم الطالب**
ID number		**الرقم الجامعي**
Section No.		**رقم الشعبة**
Serial Number		**الرقم التسلسلي**

General Instructions:

تعليمات عامة:

- Your Exam consists of 2 PAGES (except this paper)
- Phones and smart devices are forbidden inside the hall.

- عدد صفحات الامتحان 2 صفحة. (بإستثناء هذه الورقة)
- يمنع استخدام الهواتف والأجهزة الذكية داخل القاعة.

هذا الجزء خاص بأستاذ المادة

This section is ONLY for instructors.

#	Course Learning Outcomes (CLOs)	Related Question (s)	Points	Final Score
1	Describe the instruction set architecture of a MIPS processor	Q1 – Part A	5	
2	Describe the organization/operation of memory and caches	Q1 – Part B	5	
3	Describe the organization/operation of Input/Output devices	Q2 – Part A	5	
4	Analyze, develop, and test MIPS assembly language programs	Q2 – Part B	5	

Question 1: Points: 10		CLO #1, 2

Part A: Points 5 CLO #1

For **MIPS Architecture**, answer the following MCQs.

1. MIPS as a processor architecture follows which design philosophy?
   A. CISC
   B. RISC
   C. VLIW
   D. Harvard-only
2. The acronym MIPS originally stood for:
   A. Microprocessor Integrated Processing System
   B. Microprocessor without Interlocked Pipeline Stages
   C. Memory Integrated Processing Structure
   D. Machine Instruction Processing Speed
3. When MIPS is used as a performance metric, it stands for:
   A. Million Instructions Per Second
   B. Microprocessor Integrated Performance System
   C. Maximum Internal Processing Speed
   D. Memory Instructions Per Segment
4. Which of the following is TRUE about MIPS architecture?
   A. Instructions have variable length
   B. Arithmetic operations access memory directly
   C. All instructions are 32 bits long
   D. It uses only 8 registers
5. In MIPS architecture, arithmetic operations are performed:
   A. Directly on memory
   B. Between registers only
   C. Only using immediate values
   D. Only on stack

Part B: Points 5 CLO #2

6. A **14-bit address bus** can address a maximum of _____ memory locations?
   A. 4K
   B. 8K
   C. 16K
   D. 64K
7. Cache Memory acts between
   A. CPU and main memory
   B. RAM and ROM
   C. CPU and hard disk
   D. RAM and I/O
8. To speed up the performance of the processor _____ is used
   A. Timer
   B. Clock signal
   C. Pipelining
   D. Memory
9. Which of the following is fastest?
   A. Main memory (DRAM)
   B. Cache (SRAM)
   C. Hard disk
   D. Optical disk
10. Why is SRAM more expensive than DRAM?
    A. It consumes more power
    B. It requires more transistors per bit
    C. It needs refresh circuitry
    D. It is non-volatile

Question 2: Points: 10		CLO #3,4

Part A: Points 5 CLO #3

A. Describe the three main types of buses involved in I/O communication.

The three main types of buses involved in I/O communication are the address bus, data bus, and control bus.

The address bus carries the address of the memory location or I/O device that the CPU wants to access. When the CPU performs an input or output operation, it places the device or memory address on the address bus to select the correct destination.

The data bus carries the actual data being transferred between the CPU, memory, and I/O devices. It is bidirectional because data can move both to and from the CPU.

The control bus carries control and timing signals that coordinate the operation. These signals include read, write, interrupt request, interrupt acknowledgment, and bus request signals. The control bus ensures that all components act at the correct time and in the correct direction.

B. Explain the impact of increasing the size (width) of the address bus and the data bus in a computer system. Discuss how each affects system performance and capacity.

Increasing the width of the address bus increases the maximum amount of memory that the system can address.

Increasing the width of the data bus increases the amount of data that can be transferred in a single clock cycle. A wider data bus improves data throughput because more bits are moved at once between the CPU, memory, and I/O devices. This can enhance system performance, particularly in memory-intensive applications.

Part B: Points 5 CLO #4

For the assembly code of the 8086 processor shown next, answer the following multiple-choice questions.

11. How many bytes does instruction at **2000:0100** occupy?
    A. 1
    B. 2
    C. 3
    D. 4
12. What is the physical address of instruction located at 2000:0100?
    A. 20000H
    B. 20100H
    C. 21000H
    D. 20010H
13. At which address is the instruction PUSH AX stored?
    A. 2000:0105

Address (Segment:Offset)	Machine Code (Hex)	Assembly Instruction
2000:0100	B8 34 12	MOV AX,1234H
2000:0103	05 10 00	ADD AX,0010H
2000:0106	50	PUSH AX
2000:0107	BB 78 56	MOV BX,5678H
2000:010A	03 D8	ADD BX,AX

B. 2000:0106
C. 2000:0107
D. 2000:0108

14. Which instruction is 1 byte long?
    A. ADD BX,AX
    B. MOV BX,5678H
    C. INC AX
    D. JZ 0110H
15. If Zero Flag is set before executing instruction at **2000:010C**, where will execution continue?
    A. 2000:010E
    B. 2000:010F
    C. 2000:0110
    D. 2000:010D

2000:010C	74 02	JZ 0110H
2000:010E	40	INC AX
2000:010F	90	NOP
2000:0110	F4	HLT

Best Wishes

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