Taibah University		College of Computers science and Engineering
Computer Organization and Architecture COE 224		Date: 3 March 2019
Quiz: 04 Cache Memory		Total Marks: 20
Name:		ID:

1. Consider a machine with a byte addressable main memory of 2^{16} **bytes** and **block size of 8 bytes**. Assume that a **Direct mapped cache** consisting of **32 lines** is used with this machine.
   a. How is a 16-bit memory address divided into **tag**, **line number**, and **byte number**?
   b. Into what line would byte with the address **1010 1010 1010 1010** be stored?
   c. Suppose the byte with address **0001 1010 0001 1010** is stored in the cache. What are the addresses of the other bytes stored along with it?
   d. How many total bytes of memory can be stored in the cache?
   e. Why is the tag also stored in the cache?

Address = 16 bit block size = 8 ⇒ w = 3

Cache = 32 line ⇒ r = 5 bit

Address = 16 = w + r + (s − r)

s − r	r	w
8	5	3

byte No: 3 | line: 5 | tag: 8

(b) line 21

(c) 0001 1010 0001 1000 to 0001 1010 0001 1111

(d) $2^5 * 8 = 2^8 = 256$

(e)

2. Given that: Cache **access time Tc = 100 ns**
   Memory access time Tm = 500 ns
   If the effective access time is 10% greater than the cache access time, **what is the hit ratio *h***?

$T_A = hT_c + (1-h)(T_c + T_m)$

$110 = 100h + 600(1-h)$

$1.1 = h + 6 - 6h \Rightarrow 4.9 = 5h$

$h = 4.9/5 = 98\%$