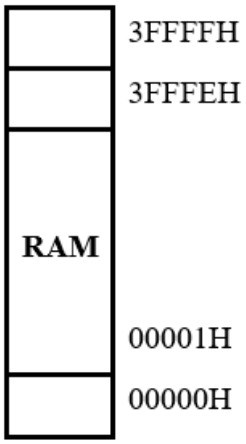
Taibah University		College of Computers science and Engineering
Computer Organization and Architecture COE 224		Date: 12 March 2019
Quiz: 01 Review		Total Marks: 30
Name:		ID:

Question 1: **[5 Marks]**

(a) Represent **+127** as **single precision floating-point** number



(b) A number that contains **3 one bits** is said to have _____ parity

(c) Assign the proper **even** parity bit to the following code: **101101011111**

_____

(d) For the shown figure of **RAM,** what is the **size of the address bus** to address the memory? _____ bit

Question 2: **[10 Marks]**

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

(a) What is the maximum directly addressable memory capacity (in bytes)?	(b) Discuss the impact on the system speed if the microprocessor bus has a 32-bit local address bus and a 16-bit local data bus, or
(c) How many bits are needed for the program counter and the instruction register?	How many instructions are there in the instruction set of this processor?

Question 3: **[5 Marks]**

Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:

INPR: Input Register, 8 bits
OUTR: Output Register, 8 bits
FGI: Input Flag, 1 bit
FGO: Output Flag, 1 bit
IEN: Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.

(a) Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.

(b) Describe how the function can be performed more efficiently by also employing IEN

Question 4: **[10 Marks]**

(a) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

(b) Consider the page stream of page requests. **2, 3, 2, 4, 6, 2, 5, 6, 1, 4, 6:** Determine the **hit ratio *h*** for this stream using the **FIFO** replacement policy, assume the main memory can hold **three pages** and initially all of them are vacant

(c) Consider a **direct-mapped** cache configuration for a byte-addressable processor. The memory size is 256 bytes. The cache has two 16-byte blocks (for a total capacity of 32 bytes). how many bits are in the **tag**, **index**, and **offset**?

(d) Give some memory addresses in which the direct-mapped cache has lowest hit rate.