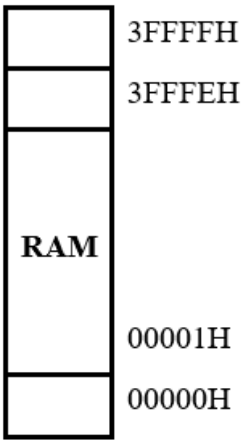
Taibah University		College of Computers science and Engineering
Computer Organization and Architecture COE 224		Date: 25 March 2019
Midterm Exam Model Ans		Total Marks: 30
Name:		ID:

Question 1: **[5 Marks]**

(a) For the shown figure of **RAM,** what is the **size of the address bus** to address the memory? 18 bit

(b) What is the total memory capacity? 256 Kbyte



Question 2: **[9 Marks]**

Consider a hypothetical 16-bit microprocessor having 16-bit instructions composed of two fields: the first 4-bit contains the opcode and the remainder the immediate operand or an operand address.

(a) What is the maximum directly addressable memory capacity (in bytes)? 4 KB

(b) How many bits are needed for the program counter and the instruction register? PC/IP: 12/16

(c) How many instructions are there in the instruction set of this processor? 16 Instructions

Question 3: **[10 Marks]**

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine

(a) How is a 16-bit memory address divided into tag, line number, and byte number?

Address = 16 bits w = 3 bits

No. of line = $32 = 2^5$ r = 5

Tag bits = 16 – 3 – 5 = 8

Tag	Line	Word
8	**5**	**3**

(b) Into what line would bytes with each of the following addresses be stored?

1010 1010 1010 1010

Line bits 1010 1

Line number = **21**

(c) How many total bytes of memory can be stored in the cache?

$Cache\ size = No.of\ line \times Block\ size$

$Cache\ size = 2^5 \times 2^3 = 2^8 = 256\ Bytes$

(d) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

0001 1010 0001 1000 through 0001 1010 0001 1111

Question 4: **[10 Marks]**

(a) Consider the page stream of page requests. **2, 3, 2, 4, 6, 2, 5, 6, 1, 4, 6:** Determine the **hit ratio *h*** for this stream using the **Least Frequently Used LFU** replacement policy, assume the main memory can hold **two pages** and initially all of them are vacant

2	**3**	**2**	**4**	**6**	**2**	**5**	**6**	**1**	**4**	**6**	
	2	2		2	2		5		1	4	
	-	3		4	6		6		6	6	

(b) A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count: Determine the effective **CPI**, **MIPS** rate, and **execution time** for this program.

Instruction Type	Instruction Count	Cycles per instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

$$Average\ CPI = \frac{45*1+32*2+15*2+8*2}{100} = \frac{155}{100} = \mathbf{1.55}$$

$$T = I_c \times CPI \times \tau$$

$$T = 100{,}000 \times 1.55 \times \frac{1}{40 \times 10^6} = \mathbf{3.875\ ms}$$

$$MIPS = \frac{f}{CPI \times 10^6} = \frac{40 \times 10^6}{1.55 \times 10^6} = \mathbf{25.8}$$